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MODELING AND DESIGN OF PRE-EQUALIZATION IN VISIBLE LIGHT COMMUNICATION

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
GAZİ UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL ELECTRONICS ENGINEERING

AUGUST 2023

ETHICAL STATEMENT

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01/08/2023

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(M. Sc. Thesis)

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ABSTRACT

In recent times, the advancements in Light Emitting Diode (LED) technology have led to increased interest in Visible Light Communication (VLC). However, the limited bandwidth of LEDs poses a challenge for achieving high transmission rates in VLC systems. To overcome this limitation, various equalization methods have been employed. However digital pre-equalizers are seen as the best option due to their simplicity and reusability. Consequently, several digital pre-equalizer methods have been proposed in the literature for VLC systems. Nevertheless, currently there is no study that investigate the implementation of digital pre-equalizers in realistic VLC systems based on the IEEE 802.15.13 standard. Hence, the purpose of this study is to propose digital pre-equalizers specifically designed in a VLC systems based on the IEEE 802.15.13 standard. The study begins by constructing a realistic channel model using signal recordings obtained from an actual 802.15.13 compliant VLC system. Subsequently, the channel model is integrated into a MATLAB based VLC system model. Two distinct digital pre-equalizers are then designed with that model. Simulation experiments are conducted to assess their effectiveness in terms of the system's Bit Error Rate (BER) performance. The results demonstrate that the proposed pre-equalizers substantially enhance the BER performance of the VLC system.

Science Code	:	90523
Key Words	:	Visible light communication, light fidelity, light emitting diode, optical wireless communication, digital pre-equalization
Page Number	:	31
Supervisor	:	Prof. Dr. Ali KARA

GÖRÜNÜR IŞIK İLETİŞİMİNDE ÖN DENGELEMENİN MODELLENMESİ VE TASARIMI

(Yüksek Lisans Tezi)

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GAZİ ÜNİVERSİTESİ

FEN BİLİMLERİ ENSTİTÜSÜ

Ağustos 2023

ÖZET

Günümüzde, Işık Yayan Diyot (LED) teknolojisindeki önemli gelişmeler nedeniyle Görünür Işık İletişimi (VLC) büyük ilgi görmektedir. Bununla birlikte, bir VLC sisteminde iletim hızını sınırlayan en önemli etmenlerden birisi kullanılan LED'lerin bant genişliğidir. Bu sınırlamayı ortadan kaldırmak için çeşitli eşitleme yöntemleri kullanılmaktadır. Bunlar arasında dijital ön ekolayzırların kullanılması, basit ve tekrar kullanılabilir yapıları nedeniyle iyi bir seçenek olmaktadır. Bu nedenle, literatürde VLC sistemleri için çeşitli dijital ön dengeleyici yöntemleri önerilmiştir. Ancak literatürde IEEE 802.15.13 standardını temel alan gerçekçi bir VLC sisteminde dijital ön dengeleyicilerin uygulanmasını inceleyen bir çalışma bulunmamaktadır. Bu nedenle bu çalışmanın amacı, IEEE 802.15.13 standardına dayalı VLC sistemleri için dijital ön dengeleyiciler önermektir. Bu amaçla öncelikle gerçek bir 802.15.13 uyumlu VLC sisteminden alınan sinyal kayıtları toplanarak gerçekçi bir kanal modeli oluşturulmuştur. Daha sonra kanal modeli MATLAB'da modellenen 802.15.13 uyumlu bir VLC algoritmasına entegre edilmiştir. Kanal modeli ile birlikte iki farklı dijital ön ekolayzır tasarımı geliştirilip anlatılmıştır. Daha sonra, kanal modeli ve dijital ön eşitleyiciler ile birlikte sistemin BER performansı açısından fizibilitesini değerlendirmek için simülasyonlar yapılmıştır. Sonuçlar, önerilen ön eşitleyicilerin VLC sisteminin BER performansını önemli ölçüde iyileştirdiğini göstermiştir.

Bilim Kodu	:	90523
Anahtar Kelimeler	:	Görünür ışık haberleşmesi, ışık veri alanı, ışık yayan diyot, optik kablosuz haberleşme, sayısal ön eşitleme
Sayfa Adedi	:	31
Danışman	:	Prof. Dr. Ali KARA

ACKNOWLEDGEMENT

I want to express my sincere gratitude to my advisor Prof. Dr. Ali KARA for her continuous support and sharing her wonderful knowledge with me. I am incredibly grateful for her patience and constructive critiques during my study. I would also like to thank my family for their patience and support throughout the study.

I would like to thank my dear manager Melike ATAY KARABALKAN, who provided me with all kinds of support during my work and did not spare her valuable comments that motivated me, and my company ELECTRA IC for providing me with all kinds of convenience.

TABLE OF CONTENTS

Page

ABSTRACT iv

ÖZET v

ACKNOWLEDGEMENTS vi

TABLE OF CONTENTS vii

LIST OF TABLES viii

LIST OF FIGURES ix

LIST OF SYMBOLS AND ABBREVIATIONS x

1. INTRODUCTION 1

2. DESCRIPTION OF THE VLC SYSTEM MODEL 5

2.1. Transmitter and Receiver Model 5

2.2. Description Of The Channel Modelling 12

3. DESCRIPTION OF THE PRE-EQUALIZER DESIGNS 15

3.1. Pre-Equalizer 1 15

3.2. Pre-Equalizer 2 16

3.3. FIR Filter 17

4. SIMULATIONS AND RESULTS 21

5. CONCULUSION 25

REFERENCES 27

CURRICULUM VITAE 31

LIST OF TABLES

Table **Page**

Table 2.1. IEEE 802.15.13 defined modulation and code rate table 8

Table 4.1. Simulation results in terms of BER 22

LIST OF FIGURES

Figure **Page**

Figure 2.1. Structure of the VLC system modeled in MATLAB 5

Figure 2.2. Structure of the transmitter model 6

Figure 2.3. Convolutional encoder generator polynomial 7

Figure 2.4. Receiver model structure 10

Figure 2.5. Illustration of fully operational VLC system 12

Figure 3.1. First pre-equalizer magnitude vs normalized frequency 16

Figure 3.2. Second pre-equalizer design model 17

Figure 3.3. Second pre-equalizer magnitude vs normalized frequency 17

Figure 3.4. Subcarrier gains of the channel and the first pre-equalizer 19

Figure 3.5. Desired vs actual filter response of pre-equalizer 1 with 201 coefficients... 20

Figure 3.6. Desired vs actual filter response of pre-equalizer 1 with 401 coefficients... 20

Figure 4.1. Constellation diagrams of 64-QAM for the VLC system:
(a) Without a pre-equalizer (b) Using first pre-equalizer
(c) Using second pre-equalizer 22

Figure 4.2. Constellation diagrams of 256-QAM for the VLC system:
(a) Without a pre-equalizer (b) Using first pre-equalizer
(c) Using second pre-equalizer 23

LIST OF SYMBOLS AND ABBREVIATIONS

The symbols and abbreviations used in this thesis are presented in below with explanations.

Abbreviations	Descriptions
ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CETS	Channel Estimation Training Sequence
CP	Cyclic Prefix
CTLE	Continuous Time Linear Equalization
DAC	Digital to Analog Converter
DCO-OFDM	DC-biased Optical OFDM
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GHz	Giga Hertz
IFFT	Inverse Fast Fourier Transform
IR	Infrared
ISI	Inter Symbol Interference
LB-PHY	Low Bandwidth OFDM Physical Layer
LED	Light Emitting Diode
LOS	Line Of Sight
MHz	Mega Hertz
OFDM	Orthogonal Frequency Division Multiplexing
O-OFDM	Optical OFDM
OWC	Optical Wireless Communication
PHY	Physical Layer
PD	Photodetector
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RC	Resistor Capacitor

1. INTRODUCTION

This chapter provides an overview of the thesis's objectives and its contributions to the literature. Furthermore, it provides a summary of the subsequent chapters and outlines the overall structure of the thesis.

Motivation

The advancement of technology has led to a growing interest in wireless communication. However, the available radio spectrum below 10 GHz is no longer sufficient [1]. Despite this limitation, Radio Frequency (RF)-based communication remains the prevailing method in wireless communication. Nevertheless, Optical Wireless Communication (OWC) has gained significant attention as an alternative solution to address this constraint. OWC utilizes the visible (VL), infrared (IR), and ultraviolet (UV) bands, which are located in the higher frequency ranges of the electromagnetic spectrum. These bands offer advantages such as license-free operation and high bandwidth [2].

Visible Light Communication (VLC) is a form of OWC that utilizes visible light as a transmission medium for data transfer. It is worth noting that the visible light spectrum falls within the range of wavelengths (380 nm to 780 nm) that are visible to the human eye as part of the electromagnetic spectrum. The use of visible light as both a means of illumination and communication offers notable benefits, such as enhanced power efficiency and cost-effectiveness compared to employing separate sources for these purposes [3, 4]. These advantages make the visible light spectrum more advantageous than other optical spectrums like infrared (IR). Furthermore, VLC offers several advantages over RF-based communication, including access to a wide unlicensed spectrum, immunity to electromagnetic interference, and enhanced security. These favorable characteristics contribute to the appeal of VLC, leading to its wide range of applications in areas such as vehicular communication [5], defense and security industries [6], underwater communication [7], internet-of-things [8], among others.

VLC employs different types of light sources, including Light Emitting Diodes (LEDs) and Laser Diodes (LDs) [9]. LEDs are predominantly utilized in various data communication

applications due to their higher reliability, enabling the demonstration of numerous data transmission scenarios [10]. While VLC offers a wide bandwidth, the achievable data rate is restricted by the bandwidth of the LEDs employed in the application. Phosphor, commonly used in lighting applications, poses a limitation on the direct modulation speed of LEDs, typically reaching around 1 MHz [11]. This bandwidth limitation primarily stems from the slower temporal response of the phosphor material [12]. To overcome this constraint, equalization methods are employed.

Essentially, there are two main types of equalization methods depending on the application side. If it is applied on transmitter side it is named as Pre-equalization and if it is applied on receiver it is named as Post-equalization. On one hand, digital pre-equalization methods have been developed employing various techniques, such as subcarrier weighting or the utilization of Finite Impulse Response (FIR) filters [13–22]. Additionally, analog pre-equalization methods have been proposed using techniques such as cascaded constant-resonance amplitude equalizers and multiple-resonant-driving equalization techniques [23, 24]. On the other hand, post-equalization methods are also commonly employed. Some analog post-equalization methods have been proposed, involving the use of constant first-order RC filters [25] or continuous-time linear equalization (CTLE) techniques with switchable response [26]. Furthermore, a combination of digital and analog post-equalization is presented, where digital FIR filters and analog RC filters are employed simultaneously [27].

The aim and contributions of this thesis

As it can be seen several equalizer methods have been proposed in the literature. However, their implementation may encounter certain difficulties. Initially, the implementation and flexibility of analog equalizer methods may pose challenges, thereby limiting their practicality and applicability[21]. Secondly, post-equalizers have disadvantages in terms of power allocation since the equalization process is performed at the receiver side. Consequently, the full scale of the Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) may not be used. In contrast, pre-equalization allows for efficient extension of LED bandwidth without compromising the received signal power, as the gain can be applied after equalization [20]. Therefore, it can be inferred that digital pre-

equalizers are the most suitable method for implementing an equalizer in a VLC system due to their straightforward and reusable structure.

Numerous digital pre-equalizer methods have been proposed for VLC systems in the literature. For instance, in one study [13], digital FIR and matched filters were employed to enhance the modulation speed of 1 MHz bandwidth white LED communication, achieving a data transmission rate of 20 Mbit/s using 4-level amplitude shift keying. Another research [14] proposed a VLC system with digital adaptive equalizers, enabling data transmission rates exceeding 100 Mbit/s. Furthermore, a power exponential software pre-equalization technique was applied in [15] to achieve higher transmission speeds, resulting in a data transmission rate of 2.08 Gbit/s over a 1-meter distance with a BER below 3.8×10^{-3}. Additionally, an automotive headlight VLC system with pre-equalization was presented in [16], achieving a data transmission rate of 427.5 Mbit/s at a distance of 1.2 meters with a BER below 3.8×10^{-5}. Moreover, a digital pre-equalization scheme using luminous feedback signal was proposed in [17] to mitigate non-linearities and low-pass effects in OFDM-based VLC systems. In [18], a straightforward method for digital pre-equalization was outlined, assessing its effectiveness by analyzing the number of time samples needed to represent each pre-equalized bit.

Another study [19] utilized a digital equalizer with square-root-raised-cosine filters and an FIR filter to compensate for LED-induced channel fading in VLC, achieving a transmission rate of 120 Mb/s with a 3-dB LED bandwidth of 13 MHz. Distributed digital pre-equalization for VLC systems based on OFDM was presented in [20], demonstrating a data transmission rate of 976.6 Mbit/s. Additionally, a pre-equalizer design based on an LED frequency response model was explored in [21], achieving a data transmission rate of 180 Mbit/s over 1.5 meters using on-off keying modulation with a BER around 10e-3. Finally, an adaptive digital pre-equalization scheme utilizing a deep learning model was proposed in [22], showing the potential to achieve high data transmission rates with a BER under 10e-6 based on experimental results.

The evaluation of digital pre-equalizers for VLC systems, as evident from existing literature, primarily focuses on BER and throughput performance in an Additive White Gaussian Noise (AWGN) channel. However, when comparing different digital pre-equalizers, it is essential to consider various factors. Firstly, to ensure a reliable assessment,

each pre-equalizer should be tested using the same algorithm. Additionally, it is crucial to maintain consistency in the test environment when comparing pre-equalizers. Moreover, while LED plays a vital role in limiting the bandwidth of a VLC system, other components such as ADC, DAC, and analog front-ends of the VLC transmitter and receiver significantly effects the channel. Therefore, to obtain more realistic results, it is advisable to investigate the performance of a digital pre-equalizer implemented in a complex algorithm that considers the frequency responses of these components in a channel. The recently approved IEEE 802.15.13 standard defines the optical wireless communication applications supporting data transmission rates of multiple Gbit/s [28]. However, there is no study in the literature that examine the implementation of pre-equalizers in a realistic VLC system based on the IEEE 802.15.13 standard.

This study aims to propose digital pre-equalizers for VLC systems based on the IEEE 802.15.13 standard. To achieve this, a comprehensive VLC system was modeled in MATLAB. After that, proposed pre-equalizers designed and tested in that model. To simulate and model a realistic VLC channel, an actual 802.15.13 compliant VLC test system was used. Initially, signal recordings were collected from this test environment and this is followed by post-processing to obtain the channel response using the Channel Estimation Training Sequence (CETS). The obtained channel response was used to implement an FIR filter, which is modeling the channel. Subsequently, the channel model was integrated into the VLC system model. Additionally, two distinct digital pre-equalizers were designed and tested on the system. Then, pre-equalizer designs was compared in terms of the BER performance. To the best of the our knowledge, this is the first literature discussion on the effects of digital pre-equalizers on a VLC system compatible with the IEEE 802.15.13 standard.

Chapters of the thesis

The rest of the thesis is structured as follows: Chapter 2 provides a description of the VLC system modeled in MATLAB, including the fundamental components of the transmitter, receiver, and channel models tailored for this system. Chapter 3 delves into the specifics of the pre-equalizers designed for the system. In Chapter 4, the simulation results are presented and analyzed. Finally, Chapter 5 offers a comprehensive conclusion to the study.

2. DESCRIPTION OF THE VLC SYSTEM MODEL

A VLC system was modeled in MATLAB to design and implement the pre-equalizer. To this end a realistic channel model was created with the records obtained from the real VLC system and it has been added on an IEEE 802.15.13 compliant algorithm. Pre-equalizer designs were made, tested and compared using this channel model.

Figure 2.1 shows a block diagram of the resulting model. As seen in the figure, the model consists of four main components: VLC transmitter model, pre-equalizer, channel model and receiver model. Each of these main components is explained in detail under separate headings.

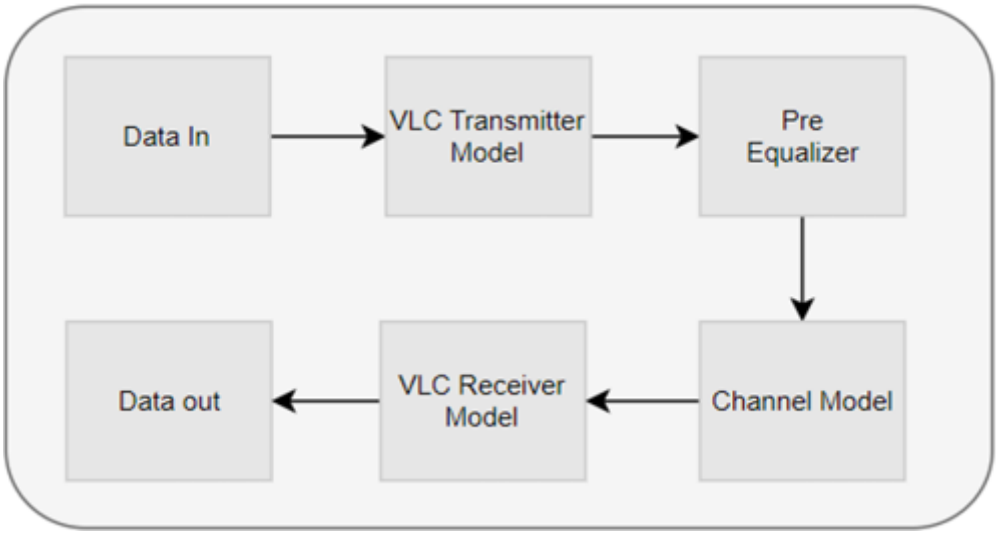


Figure 2.1. Structure of the VLC system modeled in MATLAB

2.1. Transmitter and Receiver Model

More than one PHY algorithms are presented in the IEEE 802.15.13 standard. To create the transmitter and receiver models, the DC-biased Optical OFDM (DCO-OFDM) algorithm described under the title of Low Bandwidth OFDM Physical Layer (LB-PHY) in the IEEE 802.15.13 Standard was used.

The aim of this system was to achieve data transfer rates of several Mbit/s. For this purpose, the Low Bandwidth OFDM Physical Layer (LB-PHY) algorithm defined in IEEE 802.15.13

was chosen. In the algorithm, OFDM-based modulation schemes were used. Since optical OFDM (O-OFDM) requires real-valued non-negative symbols, conventional OFDM cannot generally be used directly in VLC systems [24]. Therefore, DC-biased optical OFDM (DCO-OFDM), the default modulation scheme for LB-PHY algorithm was used in the model.

Figure 2.2 shows the structure of the transmitter model. As shown, it consists of eight stages: Convolutional Encoder, Interleaver, Modulation, Subcarrier Mapping, Channel Estimation Sequence, Inverse Fast Fourier Transform (IFFT), Frame Detection Sequence and Pulse Shaping.

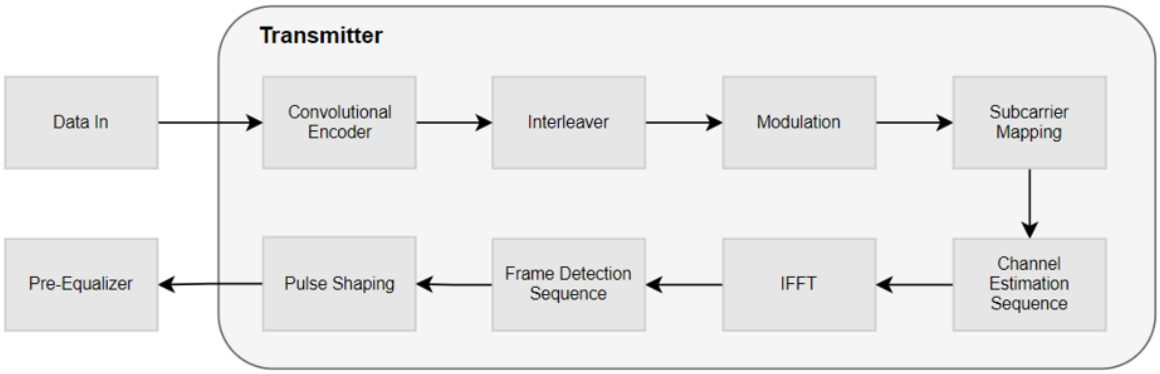


Figure 2.2. Structure of the transmitter model

Convolutional Encoder is a type of forward error correction and used for enhance the reliability of the system. In Convolutional Encoder stage, input data is encoded by a trellis structure. The data is encoded by sending more bits for each bit entered, varying with the code rate. 1/2, 2/3 and 3/4 Code Rate values are defined in the implemented IEE802.15.13 standard. There are 2 parameters to consider when choosing code rate. The first is the desired data rate, the second is the desired BER performance. Increasing the number of bits used to encode each input bit allows for greater error correction capabilities. However, this also results in a proportional reduction in the data rate. For this reason, within the defined Code Rate values, 3/4 has the best data rate value, while it offers the worst BER performance. On the other hand, 1/2 offers the best BER performance and the worst data rate value. The industry-standard generator polynomials, g0 = 133_8 and g1 = 171_8, of rate R = 1/2 is used to encode the data as shown in Figure 2.3. If higher code rates is desired, it is obtained by puncturing.

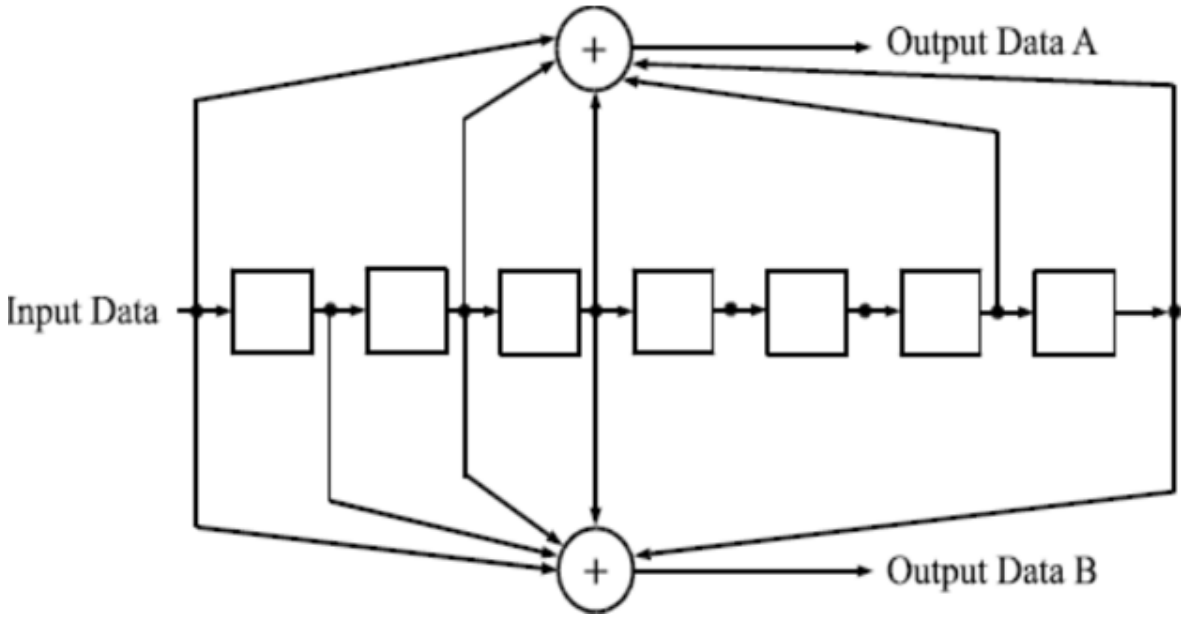


Figure 2.3. Convolutional encoder generator polynomial [28]

After the Convolutional Encoder, a block Interleaver is used. Interleaver is a method employed to reorganize the sequence of data symbols or bits in a specific pattern prior to transmitting them. All encoded bits are interleaved to spread the errors by rearranging the consecutive bits that can be influenced by distortions in the channel or the presence of noise. Therefore more reliable communication is obtained since decoders are unable to correct all the bit errors when a burst of uncorrected errors occurs.

Modulation is process of modifying a carrier signal in order to convey information or data. In the modulation stage, the data stream is modulated. IEEE 802.15.13 defines four distinct modulation types: Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), 16- QAM (Quadrature Amplitude Modulation), and 64-QAM. BPSK is the most reliable modulation type with the lowest data rate, it encompasses the process of encoding binary data by altering the phase of the carrier signal between two distinct states. QPSK is a modulation technique where the carrier signal is modified using four distinct phase states, each representing two bits of binary data per symbol. QAM is a modulation technique where the carrier signal is divided into multiple levels of amplitude and phase states. In the case of 16-QAM, there are 16 unique symbols available, with each symbol representing a specific combination of amplitude and phase. In the case of 64-QAM, there are 64 unique symbols available, with each symbol representing a specific combination of amplitude and phase. As the number of bits used to represent each symbol decreases, the performance in terms of

BER improves. However, this improvement comes at the cost of a lower data rate. In this respect, 64-QAM is the modulation type with the highest data rate but the lowest BER performance among the modulations defined in the standard.

The modulation and code rate combinations defined in the IEEE 802.15.13 standard are given in the Table 2.1. Accordingly, the fastest (highest throughput) combination is 64-QAM with 3/4 code rate, while the highest BER performance combination is BPSK with 1/2 code rate.

Table 2.1. IEEE 802.15.13 defined modulation and code rate table

Modulation	FEC Code Rate
BPSK	1/2
BPSK	3/4
QPSK	1/2
QPSK	3/4
16-QAM	1/2
16-QAM	3/4
64-QAM	2/3
64-QAM	3/4

After the modulation, modulated symbols are mapped to subcarriers at the Subcarrier-Mapping block. Subcarrier mapping is the procedure of assigning data symbols to distinct subcarriers within a multicarrier modulation system. It involves dividing the available bandwidth into multiple subcarriers and allocating each subcarrier to carry a specific part of the transmitted data. However, there are 64 subcarriers in total, in order to ensure that the output of Inverse Fast Fourier transform (IFFT) is real, Hermitian symmetry is imposed on the second half of the frame. For this reason, only 32 subcarriers are actively used. There are 24 data subcarrier, 6 zero subcarrier and 2 pilot subcarriers in the first 32 subcarrier and conjugated symmetries of them in the second half. Modulated symbols are mapped to data subcarriers of indices [3, 4, 5, 6, 8, 9, 10, 11, 12, 13 13, 14, 15, 16, 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 28], pilots are assigned to indices 7 and 21 with values of 1 and -1. Zeros are assigned to subcarrier indices [0,1,2,29,30,31]. On the other hand, Hermitian symmetric sequence of these symbols are assigned to indices between 32 and 63.

Prior to the IFFT stage, a Channel Estimation Training Sequence (CETS) consisting of two identical OFDM training symbols is appended to the signal. The role of this sequence is to facilitate the receiver in estimating the impulse response of the channel and achieving accurate fine-timing synchronization.

OFDM modulation employs an IFFT to transform the data from the frequency domain to the time domain. Since there are 64 subcarriers, 64 point IFFT is used in this module. With the OFDM technique, the input data is divided into 64 subcarriers, with each subcarrier representing a distinct frequency. Hence, each input symbols become orthogonal with each other. By this way the usage of bandwidth is decreased. So, maximum bandwidth efficiency is obtained. A guard interval called as Cyclic Prefix (CP) is added at the end of the IFFT output to eliminate the channel's multi path fading effect and to avoid inter-symbol interferences. With every OFDM symbol Last 16 subcarrier is added to end of the module. Therefore, thanks to CP, efficiencies have decreased but ISI performance has increased.

After the IFFT, the Frame Detection Sequence (Preamble) is added at the beginning of each OFDM symbol to be used for packet detection and synchronization at the receiver. Preamble consists of 640 samples that are spread in two OFDM symbol time. 640 samples are generated by using two original PN sequence with length of 20 bits. Firstly, both sequences are up-sampled by 8. Then, two up-sampled data sequences with length of 160 are filtered As a result, Preamble sequence is created by concatenated two up-sampled and filtered PN sequences (160+160) and their flipped versions.

In Pulse Shaping Filter stage, the data is upsampled by a factor of 8 and filtered before the ADC process. Pulse Shaping Filter is used to shape the transmitted signal to ensure that signal has the specified signal properties and bandwidth constraints. Hence, Inter Symbol Interference (ISI) is reduced and Signal to Noise Ratio (SNR) is getting better by filtering the transmitter data.

Figure 3 depicts the structure of the receiver model structure. Receiver model consists of 10 blocks named Packet Detection, Match Filter, Symbol Timing, FFT, Channel Estimation, Channel Equalizer, Subcarrier Demapping, Demodulation, Deinterleaver and Viterbi Decoder.

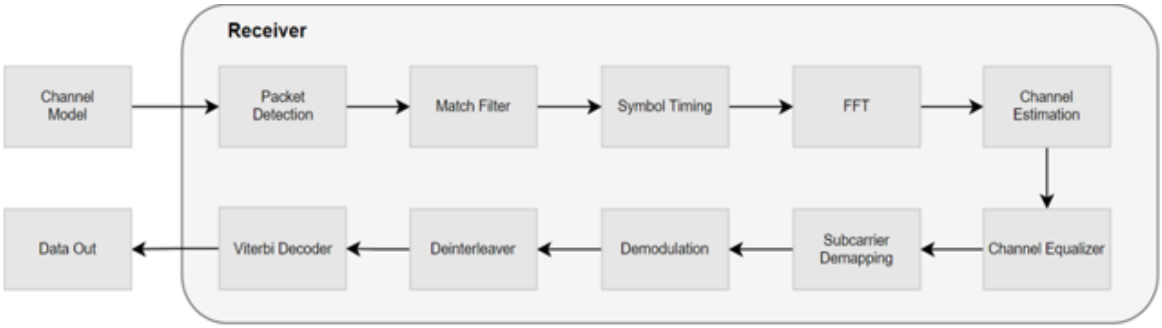


Figure 2.4. Receiver model structure

The first block in the receiver model is Packet Detection, the data from the channel model is first sent to the Packet Detection block. As mentioned in Transmitter, a Frame Detection Sequence is added to the beginning of the packet when transmitting the packets. Primary duty of the Packet Detection block is finding to starting point of the packet by using original Frame Detection Sequence. Packet Detection block works continuously until packet detection is succeeded.

When a packet is detected, this packet sourced the Match Filter which shares the same characteristics as the Transmitter Pulse Shaping filter. The purpose of the Match Filter matches the shape and characteristics of the transmitted signal identify. Hence transmitted signal is corrected from the received signal that may be noisy Signal to Noise Ratio is increased. Following the filtering of the incoming stream, it proceeds the Symbol Timing block.

The Symbol Timing stage serves two purposes which are down sampling and frame detection. Initially, the data is down-sampled by a factor of 8 using the maximum output energy method, which estimates the sampling points for each symbol. The down-sampled signals transferred to the Frame Detection process, which includes synchronizing the OFDM symbols within a packet. This is achieved by evaluating the cross-correlation of Channel Estimation Training Sequence. The outcome of the correlation reveals the start and end points of an OFDM symbol. To perform the cross-correlation operation, a FIR filter with 160 taps (coefficients) is implemented where a portion (400) of the received signal serves as the input. Consequently, after the Symbol Timing stage, synchronization within a packet is successfully accomplished.

After the received signal is captured and down-sampled, it is passed from the frequency domain to the time domain again in the FFT block. At this stage, the Cyclic Prefix data, which was previously added in the transmitter, is removed from the OFDM symbol, resulting in the retrieval of the original 64 subcarriers. Subsequently, the 64-point Fast Fourier Transform (FFT) process is applied. After the OFDM Demodulation process is done data is sourced the Channel Estimation or Channel Equalizer blocks.

The received signals are distorted due to various factors in the channel. In order to recover the received bits from the channel effect, it is estimated in Channel Estimation block and compensated in Channel Equalizer block. CETS consists of a 2 OFDM symbol long signal sent by the transmitter by adding the beginning of the OFDM symbol after the preamble. Using this training sequence, the channel response is calculated in the Channel Estimation block. Each subcarrier component of the received signal can be expressed as sum of the transmitted signal and channel effect at that subcarrier thanks to the orthogonality of OFDM modulation. Therefore, the transmitted signal can be recovered by estimating the channel response just at each subcarrier. To achieve this, channel response of each subcarrier is estimated using CETS and then this response fed to the Channel Equalizer block.

Division/multiplication procedure is employed in Channel Equalizer block to equalize the OFDM-demodulated signals. The estimated channel frequency response, which represents the inverse response of the channel, is multiplied by the frequency domain OFDM symbols. As a result, the influence of the channel on the received symbol is effectively eliminated.

Following the FFT process, the subcarriers are converted back to the time domain, and the channel's impact is mitigated. So, these subcarriers demapped back with the same way which was defined in the Subcarrier Mapping section, which is then forwarded to the demodulation block.

In the demodulation block, the original data is taken from the modulated carrier signal. Demodulation uses the inverse modulation technique used in the transmitter to correctly decode the transmitted bits. By demodulating the received signal, the encoded information is recovered from the disturbance effects of the channel. After the Demodulation block complex data symbols are demodulated and sourced to Deinterleaver block.

Deinterleaving aims to reverse the interleaving process applied at the transmitter, thereby restoring the original order of received symbols or bits. When the deinterleaver process is done, data is rearranged in its initial sequence and ready to decode. After deinterleave process is done, bitstream is sourced to Viterbi Decoder block.

Viterbi Decoder block is used to decodes the bitstream which was encoded in the transmitter with using same polynomial generator to create Trellis Structure. Viterbi Decoder analyze the received signal and determine the most probable transmitted sequence among all possible options using the Trellis structure. Thus, the errors that occur in the received signal are tried to be minimized.

2.2. Description Of The Channel Modelling

To create a channel model, the first step involved gathering real signal recordings from a VLC system that complies with the IEEE 802.15.13 standard. The system, illustrated in Figure 4, comprises a PHY transmitter (FPGA), a Digital-to-Analog Converter (DAC), a VLC transmitter, an LED, a channel, a photodetector (PD), a VLC receiver, an Analog-to-Digital Converter (ADC), and a PHY receiver (FPGA).

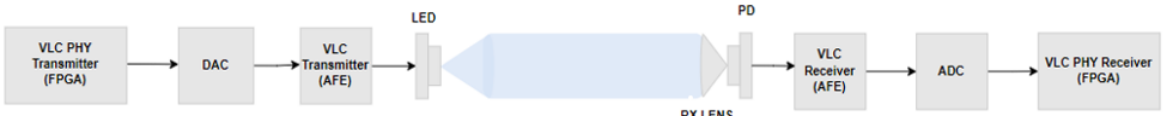


Figure 2.5. Illustration of fully operational VLC system.

VLC PHY Transmitter contains VLC PHY Transmitter algorithm blocks and implemented on an FPGA. Input data stream is processed in VLC PHY Transmitter and then sourced to DAC for digital to analog conversion. The VLC Transmitter is used to drive the LED with the maximum achievable amplitude within its linear range. To achieve this, the signal from the DAC is amplified, which followed by the application of a Bias Tee.

It is crucial to acknowledge that the data after the VLC PHY Transmitter has real values as a result of Hermitian symmetry. Nevertheless, since the data still bipolar, it is not suitable to modulate a LED. To address this, a DC bias is added to the data. This bias serves two purposes: first, it shifts the negative values to positive, and second, it allows the LED to

operate within its linear region prior to modulation of the LED intensity. Once the DC bias is applied, the signal after the DAC is transmitted using visible light with the aid of the LED.

LED and PD are fixed in height and distance in the test environment. Therefore, a Line Of Sight (LOS) Channel is achieved in the system between the LED and PD. Consequently, the signal converted to visible light by the LED and it is transmitted through the LOS channel. On the receiver side, PD captures the signal which is coming from the channel and converts it to current. The VLC Receiver contains a Transimpedance Amplifier (TIA) in it, thus it converts current to voltage and feeds this signal to the ADC. The ADC converts this analog signal to digital, so that the signal can be processed by the VLC PHY Receiver. VLC PHY Receiver contains VLC PHY Receiver algorithm blocks and it is implemented on an FPGA similar as the VLC PHY Transmitter.

It is important to mention that the ADC and DAC were configured with a sampling frequency of 200 MHz. Considering that the up-sampling rate of the transmitter model algorithm was set to 8, a 25 MHz bandwidth was selected for implementation in the system. On the other hand, reading light type LED was employed in the test system and bandwidth of this LED is calculated as 4 MHz. For this reason, it has been observed that the most limiting element of the bandwidth in the channel is the LED.

Although the LED is the most important factor limiting the bandwidth in the channel, there are many other factors. Response of the channel can be examined in three parts as Transmitter, Receiver and Air. In this case, the Transmitter Response, $H_T(f)$, consists of DAC, LED and VLC Transmitter responses.

$$H_T(f) = H_{DAC}(f)H_{LED}(f)H_{TX}(f) \tag{2.1}$$

Receiver Response, $H_R(f)$, consists of ADC, PD and VLC Receiver responses.

$$H_R(f) = H_{ADC}(f)H_{PD}(f)H_{RX}(f) \tag{2.2}$$

When the effect of the Air $H_A(f)$ is added to the Transmitter and Receiver responses, the total channel response $H(f)$ can be expressed as follows:

$$H(f) = H_T(f)H_A(f)H_R(f) \tag{2.3}$$

To model the total channel response of the test system, signal after the ADC is recorded before being processed in the VLC PHY Receiver. Thus, the effect of all components in the system such as DAC, LED, VLC Transmitter, Channel, PD, VLC Receiver can be observed on the transmitted signal.

Once the recordings were collected, they were post-processed in MATLAB to obtain the channel response of the system using the Channel Estimation Training Sequence (CETS). Specifically, the CETS comprised 2 OFDM symbols that allowed for the observation of the disruptive effects caused by the channel. It is important to note that the algorithm in the system has 64 subcarriers. However, only the gain of the first 32 subcarriers was employed to construct the channel model since the subcarriers are Hermitian Symmetric. The gain of each subcarrier was determined by averaging the gain of the 2 OFDM symbols. These calculated gains were then used to create a channel response model, which is a 401-tap FIR filter. Finally, the channel model was integrated into the VLC system model and used to design and test pre-equalizers.

3. DESCRIPTION OF THE PRE-EQUALIZER DESIGNS

Two different pre-equalizer designs were made using the VLC system model. In this section, these pre-equalizer designs will be explained. The primary objective of Pre-Equalizer designs is to eliminate the disruptive impacts of the channel by applying the inverse of the channel response. Once the channel response $H(f)$ is obtained, then the frequency response of the pre-equalizer $H_P(f)$ can be approximated as

$$H_P(f) \cong 1/H(f) \tag{3.1}$$

Then, the overall system response can be written as

$$S_R(f) = S(f)H(f)H_P(f) \tag{3.2}$$

where $S(f)$ is the desired response while $S_R(f)$ is the received response after the pre-equalization. As seen here, while a perfectly estimated channel response and an impeccably constructed pre-equalizer can eliminate all channel effects perfectly, achieving this level of perfection is nearly impossible in practice, particularly in multi-carrier systems. In this context, two FIR-based pre-equalizers are designed to demonstrate that channel effects are greatly reduced within a fully functional VLC system, which operates as a multi-carrier system.

3.1. Pre-Equalizer 1

The primary concept behind the first pre-equalizer was to utilize the inverse of the gain responses for each subcarrier, which could be derived from the Channel Estimation Training Sequence (CETS). In the pre-equalizer 1 design, the same method used to create the channel model was repeated using the inverse of the channel frequency response.

In this regard, once the modeled channel was integrated between the transmitter and receiver within the VLC system model, data transfer was initiated by the transmitter and the Channel Estimation Training Sequence was extracted and recorded at the receiver. Then, the channel response for each subcarrier was extracted using the Channel Estimation Training Sequence

recording. Thus, the pre-equalizer design consisting of 201 taps was completed, using the inverse of the channel response that is the expected output response of the pre-equalizer design.

Normalized frequency vs magnitude graphic of the first equalizer is shown in the Figure 3.1. Since 200 MHz sampling frequency was used with 8 upsampling in the test environment, 200 MHz was also used in filter designs (25 MHz bandwidth). The inverse of the frequency response of the 32 subcarriers obtained from Channel Estimation Training Sequence is used, while the remaining frequency ranges are filled with a value of 1 as it is unimportant for the study.

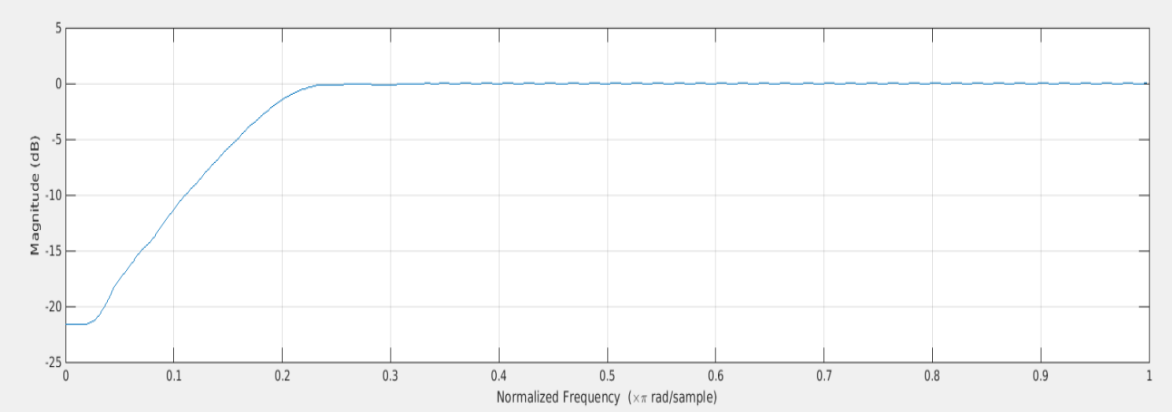


Figure 3.1. First pre-equalizer magnitude vs normalized frequency

3.2. Pre-Equalizer 2

Design process of the second pre-equalizer is shown in the Figure 3.2. As shown in the figure, second pre-equalizer is designed using single tone sinusoidal signals with a frequency range of 1 MHz to 25 MHz with 1 MHz increments. These sinusoidal signals were transmitted through the channel within the VLC system model. A Fast Fourier Transform (FFT) procedure was then applied to the signals received from the channel, allowing for the extraction of the amplitude value associated with the corresponding frequency. Thus, the maximum amplitudes obtained for each frequency were normalized and the frequency response of the channel in the relevant bandwidth was calculated. Thus, the pre-equalizer design consisting of 201 taps was completed, using the inverse of the channel response that is the expected output response of the pre-equalizer design.

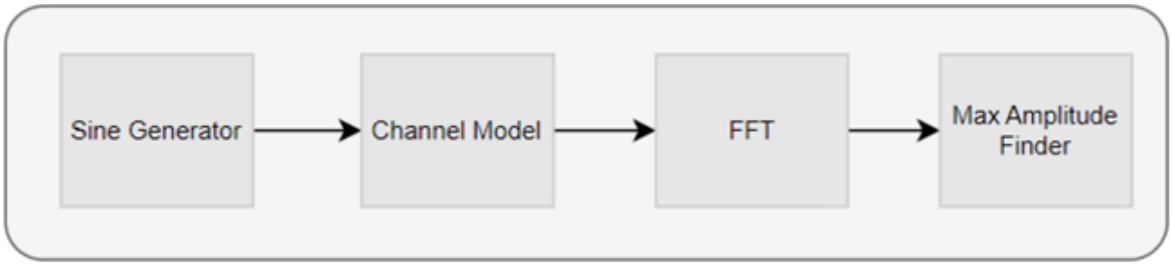


Figure 3.2. Second pre-equalizer design model

Normalized frequency vs magnitude graphic of the second equalizer is shown in the Figure 3.3. As described in the first pre-equalizer, 200 MHz frequency sampling rate is used in the filter design. The effect of attenuating the sinusoidals between 1-25 MHz of the channel obtained as a result of the measurements was taken inversely and used in the filter design, while the remaining frequency ranges are filled with a value of 1 as it is falls outside the targeted bandwidth.

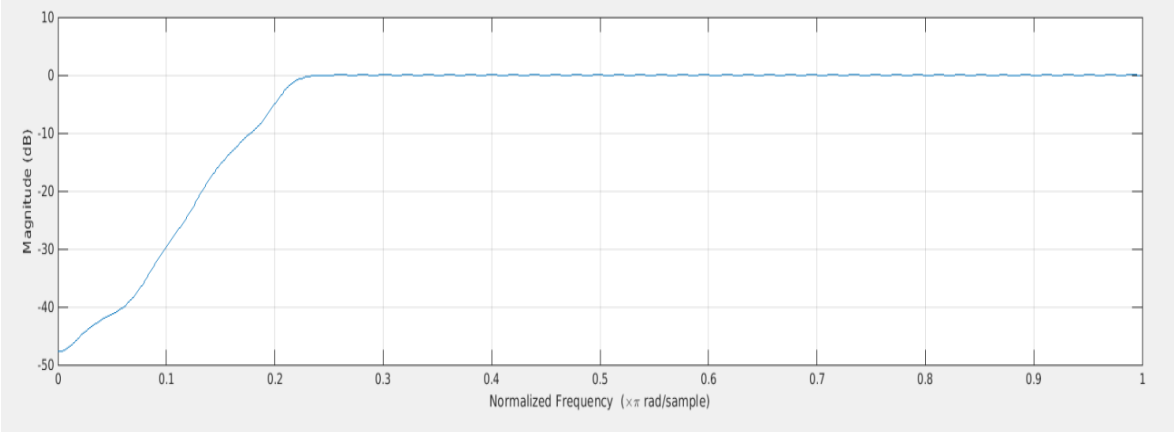


Figure 3.3. First pre-equalizer magnitude vs normalized frequency

3.3. FIR Filter

The pre-equalizer designs and channel model used in the study were realized using digital filters. There are 2 commonly used filter types in communication, Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) Filter.

Because feedback is not present in FIR filters, they can only operates on current and previous input values. However, the IIR filter works with not only the current and previous inputs, but also the previous output sample. Therefore, although FIR filters require more memory

usage and processing power than IIR filters, they were preferred in this study due to their linear phase filtering features and more stable operation.

The FIR filter is a fundamental element in digital signal processing. It consists of a finite sequence of coefficients that define its impulse response [29]. The relationship between the input and output of an FIR system is expressed by the following equation:

$$\mathrm{y[n]} = \sum_{k=0}^{N-1} h(k)\mathrm{x(n-k)} \tag{3.3}$$

Hence FIR filter system function is:

$$\mathrm{H(z)} = \frac{Y(z)}{X(z)} \sum_{n=0}^{N-1} h(n) z^{-n} \tag{3.4}$$

The objective of pre-equalizer designs is to achieve a frequency response that counteracts the disruptive effect of the channel. To achieve this, it is first necessary to find the frequency response of the channel. For this reason, in both filter designs, the channel response was first found with different methods, and then the filter was designed using the inverse of the channel frequency response. Therefore, even though the two filters want to reach the same point, the main difference between the proposed filter designs is how the channel response is found.

Figure 3.4 presents a comparison between the normalized gain responses of the first 32 subcarriers in the channel model and the first pre-equalizer. The figure clearly illustrates that the channel model response is exactly inverse of the pre-equalizer response and in this context, channel model acts as a low-pass filter, while the pre-equalizer act as a high-pass filter.

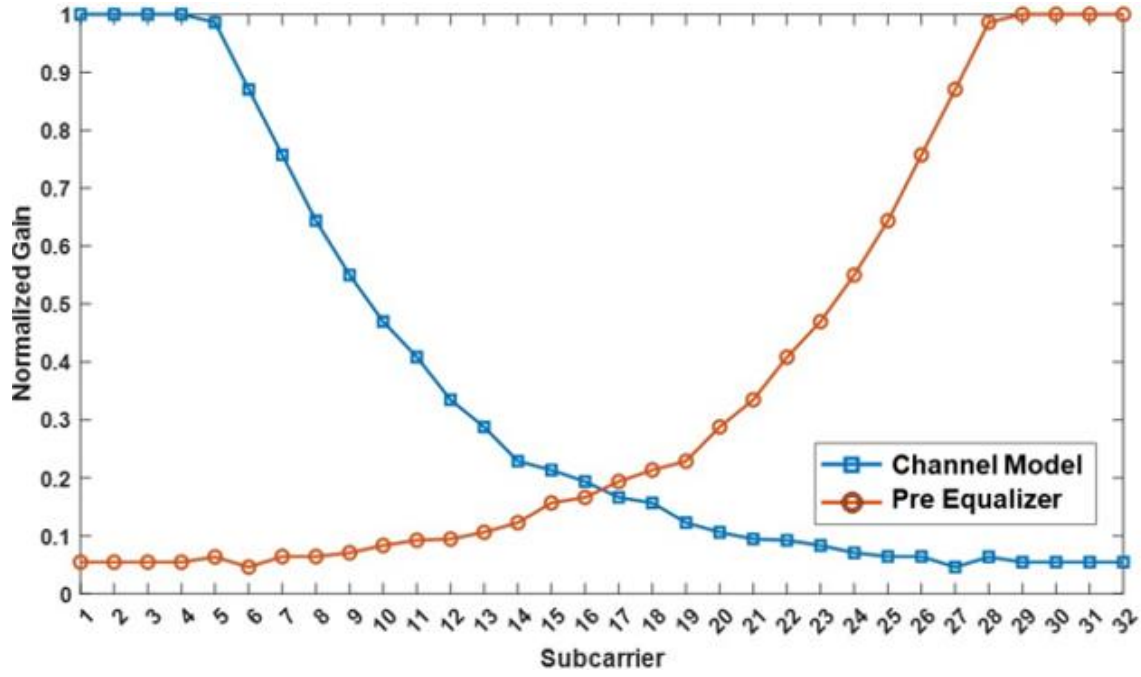


Figure 3.4. Subcarrier gains of the channel and the first pre-equalizer

The two most important factors affecting the filter design are sampling frequency and coefficient number. Since the sampling frequency of the system used to create the channel model is 200 MHz, it was chosen as 200 MHz in the pre-equalizer designs. On the other hand, pre-equalizer designs were designed using 201 tap, that is, 201 coefficients. Although increasing the number of taps allows the filter to give a more ideal result, it increases the design complexity and resource usage. For this reason, the trade-off between resource usage and filter sharpness should be carefully evaluated in proposed pre-equalizer designs made with the FIR filter method.

While designing the filters, all frequencies from zero to half of the sampling frequency value were divided into equal intervals named filter coefficients. For all frequencies in this range, coefficients were calculated by entering the desired value (using channel response) at the filter output for the relevant frequency.

Normalized frequency vs magnitude graphs of two filters with 201 tap numbers in Figure 3.5 and 401 taps in Figure 3.6 are shared. The desired response and the frequency graphs of the designed filters are shown in the figures. As shown in the figures, as the number of taps increases, the filter response gets closer to the desired one.

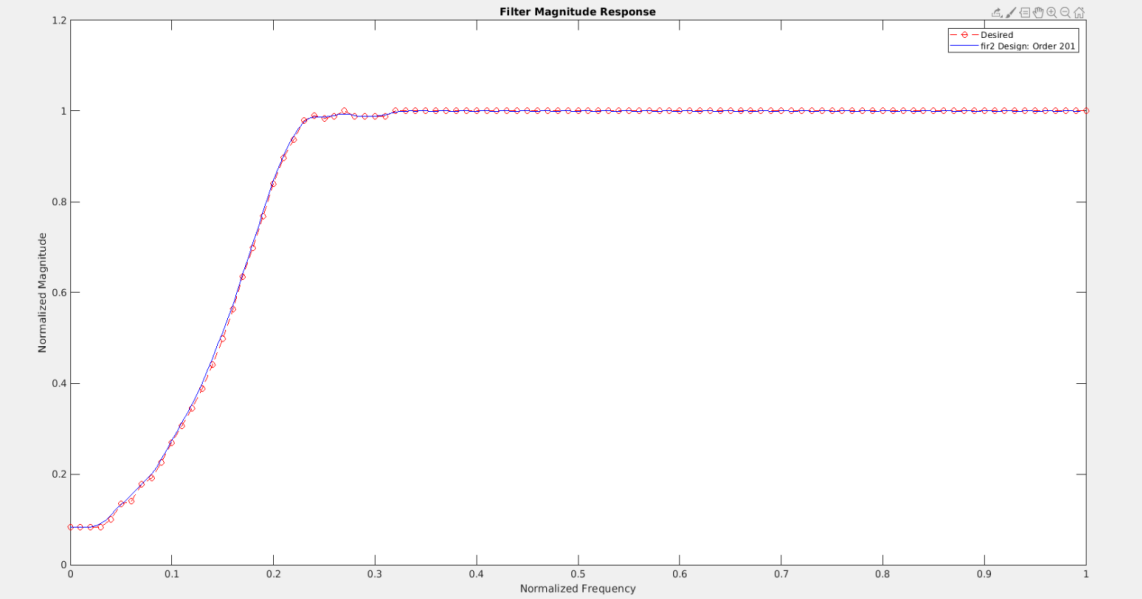


Figure 3.5. Desired vs actual filter response of pre-equalizer 1 with 201 coefficients

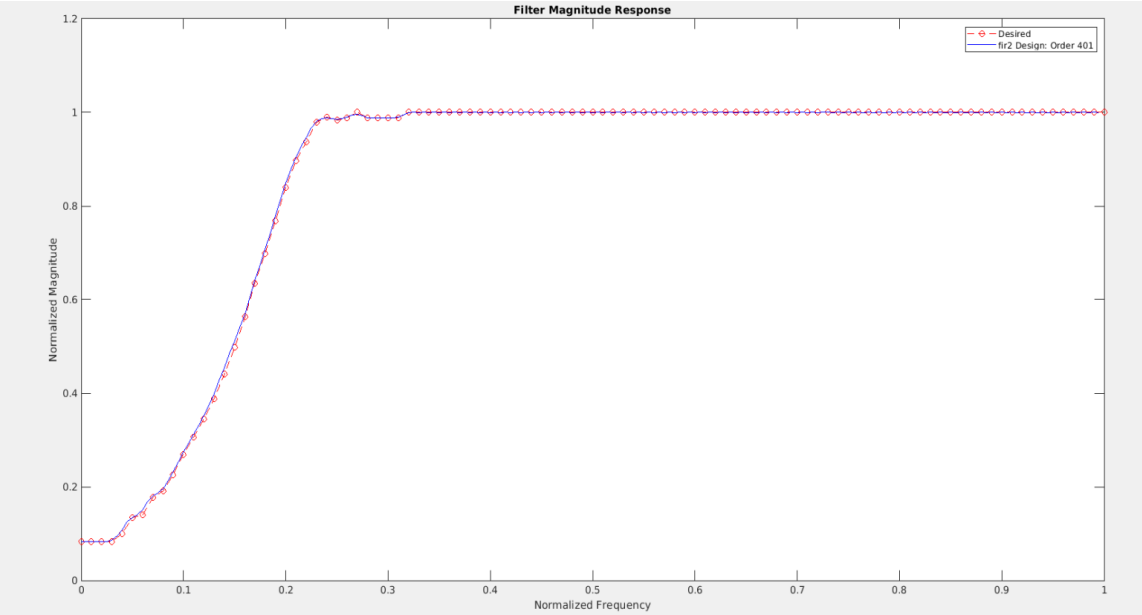


Figure 3.6. Desired vs actual filter response of pre-equalizer 1 with 401 coefficients

4. SIMULATIONS AND RESULTS

The proposed pre-equalizer designs were tested on the VLC system model which described in the previous sections. Proposed pre-equalizer designs placed between the channel model and transmitter, after that simulations were conducted in MATLAB and their performances are compared in terms of BER. In the simulations, a random bitstream was generated with the maximum packet size specified in the IEEE 802.13.15 standard (2047 bytes). Then, this bitstream transmitted from the VLC PHY transmitter model to the proposed pre-equalizer filters. Subsequently, the subcarriers were equalized based on their frequency response and amplified 16 times before being sent to the channel. The resulting data was then processed by the VLC PHY receiver model. Finally, a BER analysis was executed to the data from the receiver. In order to obtain a realistic result, simulations were repeated 1000 times for both the VLC system with and without the pre-equalizer designs.

Conversely, the LB-PHY algorithm outlined in the IEEE 802.15.13 standard support the utilization of BPSK, QPSK, 16-QAM, and 64-QAM modulation schemes. Among these options, 64-QAM was selected for the simulations due to its superior bandwidth efficiency in comparison to lower-order QAMs. Thus, it was desired to observe the performance of pre-equalizer designs more clearly by obtaining higher BER values. Additionally, to assess the viability of the proposed pre-equalizers with higher-order QAMs, 256-QAM was employed in the simulations, despite not being supported by the standard. Throughout the simulations, a fixed code rate of 3/4 which is supported by IEEE 802.15.13 standard as well, was maintained to ensure consistency.

Table 1 presents the experimental results regarding the BER. Additionally, Figure 6a, Figure 6b, and Figure 6c shows the constellation diagrams of 64-QAM for the VLC system without a pre-equalizer, with the first pre-equalizer, and with the second pre-equalizer, respectively. Similarly, Figure 7a, Figure 7b, and Figure 7c display the constellation diagrams of 256-QAM for the VLC system without a pre-equalizer, with the first pre-equalizer, and with the second pre-equalizer, correspondingly.

Table 4.1 . Simulation results in terms of BER

System	BER - QAM-64	BER - QAM-256
Without Pre-Equalizer	19900e-5	35000e-5
First Pre-Equalizer	0,438e-5	2700e-5
Second Pre-Equalizer	0	6,65e-5

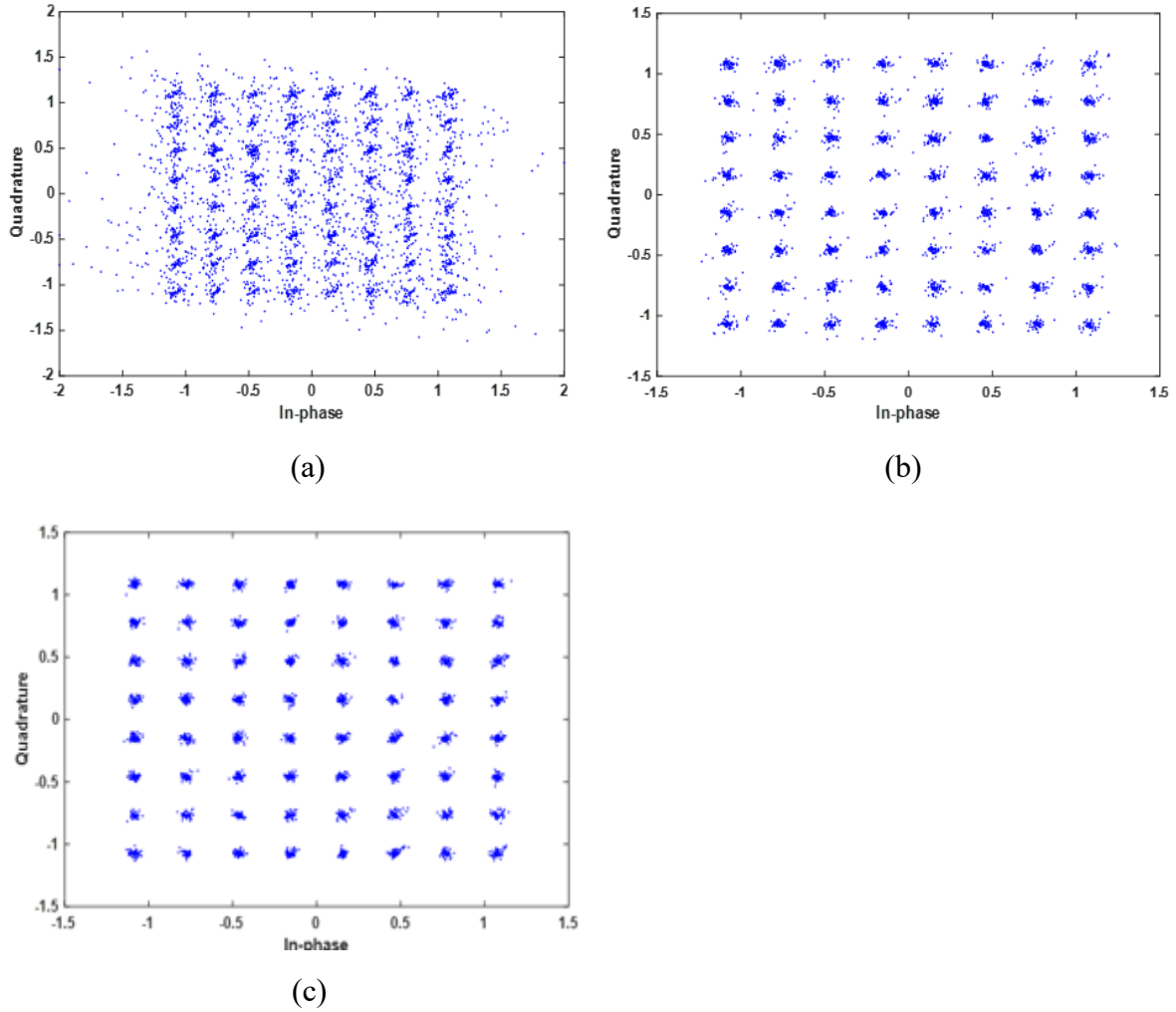
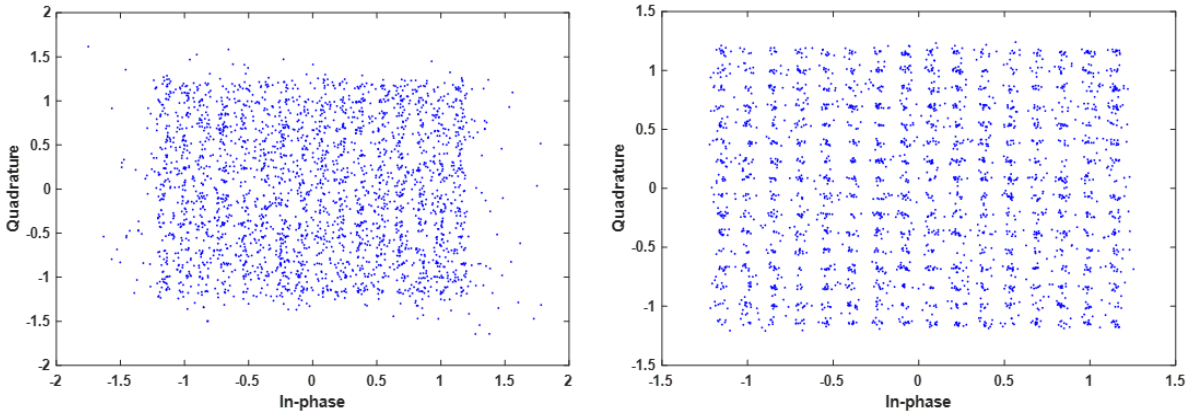
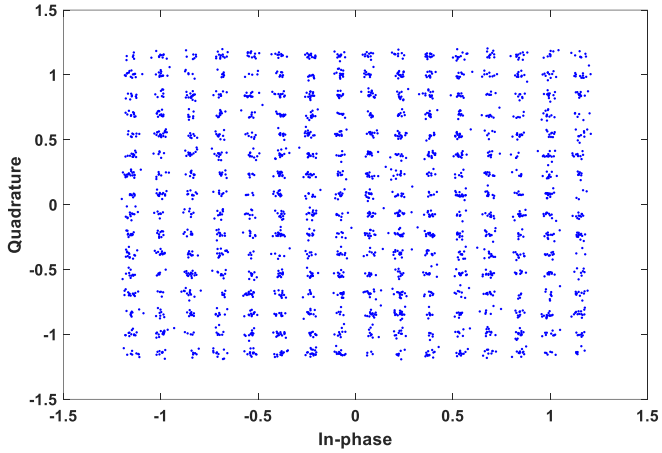


Figure 4.1 . Constellation diagrams of 64-QAM for the VLC system: (a) Without a pre-equalizer (b) Using first pre-equalizer (c) Using second pre-equalizer.



(a)

(b)



(c)

Figure 4.2. Constellation diagrams of 256-QAM for the VLC system: (a) Without a pre-equalizer (b) Using first pre-equalizer (c) Using second pre-equalizer

The simulation results can be analyzed from two perspectives: (1) the impact of the proposed pre-equalizers on the system's BER performance by comparing VLC system with and without pre-equalizer, and (2) the BER performance of the proposed equalizers by comparing VLC system with pre-equalizer design 1 and VLC system with pre-equalizer design 2 using bandwidth-efficient modulation schemes such as 64-QAM and 256-QAM. Examining the results presented in Table 1 reveals that the system's BER performance is significantly compromised when operating without a pre-equalizer, particularly under higher-order QAM schemes. Specifically, the BER values for the system without pre-equalizers are 19900e-5 for 64-QAM and 35000e-5 for 256-QAM. However, the proposed pre-equalizers substantially enhances the system's BER performance.

Table 1 demonstrates that when using the 64-QAM, the system's BER value with the first equalizer is recorded as 0,438e-5. Conversely, when employing 256-QAM, the system's BER value significantly decreases with the first equalizer to 2700e-5. Despite this reduction, the attained BER performance remains within acceptable limits, which enabling the using of the first equalizer for 256-QAM signals.

In contrast, when considering the system with the second equalizer, a BER of 0 is obtained for 64-QAM, whereas a BER of 6,65e-5 is achieved for 256-QAM. These results indicate that the system with the second equalizer maintains satisfactory BER performance even when operating with a higher-order QAM modulation scheme. Consequently, it is evident that the system incorporating the second pre-equalizer outperforms the system utilizing the first equalizer in terms of BER performance.

The simulation results demonstrate a significant enhancement in the BER performance of the VLC system through both pre-equalizer designs. Nevertheless, additional considerations are required to address the limitations associated with the design of the proposed pre-equalizers.

5. CONCULUSION

Although the simulation results provide important evidence about the achievements of pre-equalizer designs against the disruptive effect of the channel, the design phase may present certain challenges and complexities. While summarizing the study through the results and the design phase, this section aims to provide a brief discussion of these concerns, providing valuable information that may be vital when making decisions during the design of the proposed pre-equalizers.

During the design phase of the first pre-equalizer, an important consideration arises regarding the utilization of the Channel Estimation Training Sequence to obtain the inverse of the gain responses for each subcarrier. This necessitates the implementation of a post-processing approach. In this approach, the received signals (recordings) are processed in a software environment such as MATLAB, employing packet detection symbol timing and FFT (OFDM Demodulation) algorithms to eliminate the Channel Estimation Training Sequence from the recordings.

Alternatively, instead of post-processing, it is possible to integrate the same algorithms into the PHY algorithm as an extension on hardware, such as an FPGA, to calculate the filter coefficients. This would result in a dynamic pre-equalizer capable of easily computing the filter coefficients, even when the transmission channel undergoes changes. However, the practical implementation of this approach may present challenges in terms of design time and resource usage. Therefore, using the post-processing approach is more straightforward and the cheapest solution than the hardware implementation that is likely to be preferred for the design of the first pre-equalizer.

As the design of the second pre-equalizer relies on the utilization of sinusoidal signals, there is no need for a post-processing step or hardware implementation. Consequently, the second pre-equalizer can be implemented using the recorded signals obtained from a test setup. Therefore, while designing the second pre-equalizer it is necessary to construct a testing environment or measurement setup to calculate the frequency response of the channel. However, it should be noted that achieving a dynamic structure for the pre-equalizer is not feasible in this case. Consequently, when the transmission channel undergoes changes,

measurements should be repeated using test setup and the filter coefficients must be recalculated.

In summary, both of the suggested pre-equalizers lead to a substantial enhancement in the system's BER performance. However, it can be inferred that while the second pre-equalizer offers lower BER in the VLC system, its design and implementation may come with higher costs. On the other hand, the first design can be chosen for the VLC system, despite relatively higher BERs. It is worth mentioning that the first design can employ the post-process approach for simplicity during its design phase.

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Gazili olmak ayrıcalıktır