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Distribution of interface traps in Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structures

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ABSTRACT: This study presents voltage-dependent profile of interface traps in Au/*n*-Si structure with 2% graphene–cobalt-doped $Ca_3Co_4Ga_{0.001}O_x$ interfacial layer. Admittance measurements revealed capacitance-voltage (C-V) plots with typical regions of a metal–insulator–semiconductor structure through inversion, depletion, and accumulation regions. Frequency dispersion is observed in C-V plots and such behavior was explained with excess capacitance, which is associated with the density of interface traps (D_{it}) in the structure because larger D_{it} is observed when the measurements are held at low frequencies due to the fact that traps can follow the signal depending on their lifetime. D_{it} was also obtained using conductance method, which also provided lifetime of the traps. The difference between the values of D_{it} was attributed to the difference in extraction methods. Obtained results showed that Au/2% graphene–cobalt-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure yields promising electrical characteristics when the structure is operated at high frequencies. © 2019 Wiley Periodicals, Inc. J. Appl. Polym. Sci. **2020**, *137*, 48399.

KEYWORDS: density of interface traps; depletion capacitance; graphene; parallel conductance

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INTRODUCTION

When a metal/semiconductor interface of a Schottky device is filled with a sufficiently thick insulator interlayer, the new structure still keeps the feature of a Schottky contact, whereas this insulator interlayer also gives the structure the property of a capacitor, which stores electric charges. Early studies on silicon-based structures mostly utilized SiO_2 due to its conformity. Nevertheless, the quest for new interlayer materials still continues for purposes such as surface passivation, barrier height modification, leakage current minimization, and so on. Therefore, recently, some researchers focus on improvement of the performance or quality of these devices especially by using polymeric interlayer materials due to their high surface area to volume rate, low cost, low weight, good mechanical strength, charge storage capacity, flexibility, high dielectric strength, and their suitability to easy preparation methods such as electrospinning, solid–liquid phase separation, and template synthesis.[1–8] Owing to these unique properties of polymeric materials, metal–polymer–semiconductor (MPS) structures have become an attractive research topic for physicists, chemists, and electrical and electronics engineers as well. Polymers that are fabricated with electrospinning method comprise the large part of studies in the literature. In the last decade, there has been a growing interest toward electronic devices such as Schottky barrier diodes that are comprised of electrospun polymeric layer[1,2,4,7,8] as well as other applications such as blood filtration, wound dressing, oil–water separation and alike.[9–11]

It is well known that the formation of an interlayer (native or deposited), the origin of D_{it}, and series resistance (R_s) can cause deviation from the ideal case.[12–14] In general, D_{it} occurs due to the interruption of the periodic lattice structure of the surface, surface preparation, the interfacial layer and its homogeneity, impurity concentration of semiconductor, and the organic pollution in the laboratory environment.[10–15] The frequency dependence is related to the characteristic trap response time ($\tau = 2\pi/\omega$), where ω is the angular frequency. The recombination losses at a semiconductor surface can be diminished by the reduction in the number of defects at the interface and reaching surface passivation is based on a significant reduction of the electron or hole concentration at the semiconductor interface by means of a built-in electric field.[13–16] In other words, a high-dielectric material as interlayer at M/S interface can yield an excellent surface passivation properties on semiconductor crystal, which is of vital importance for device applications such as Schottky type MIS diodes/photodiodes and the structures in which metal and semiconductor are separated by an interlayer.

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These traps have an energy distribution within the forbidden bandgap (E_g) and even extend into the conduction band (for n-type) or valence band (for p-type) of the semiconductor.

It is expected that the value of capacitance increases with increasing voltage at weak inversion, depletion, and weak accumulation regions, but experimental results may suggest otherwise due to the existence of these interface traps. Because electronic charges (electrons or holes) are trapped in these states and they will act like positive or negative charges at the interface.[12–16] There are several techniques employed to measure and characterize the D_{it} in Schottky type structures.[15,16] However, the most sensitive, accurate, and reliable method is the conductance method which is proposed by Nicollian and Goetzberger.[16] On the other hand, this method has a disadvantage of being quite laborious and time consuming. The high–low frequency (C_{HF}-C_{LF}) capacitance method developed by Castagne and Vapaille[17] and forward bias current–voltage (I-V) method developed by Card and Rhoderick are also appropriate methods in terms of being simple.

Conductance method can be used to measure of D_{it} values on the order of 10^9 $eV^{-1}.cm^{-2}$ and it does not only extract the values of D_{it} in the depletion and weak inversion regions, it is also possible to obtain the capture cross section (σ_p) and relaxation time (τ) of the states as well as the fluctuation of the surface potential (ψ). This method is based on measuring the C_m and G_m of the structure both as a function of voltage and frequency. The value of G_p/ω represents the loss mechanisms occurring when traps capture or emit carriers. In order to extract the D_{it} value, the values of C and G are measured as a function of frequency and they are used to calculate G_p/ω.[14,16] When G_p/ω is plotted against angular frequency, the value of G_p/ω versus ω will exhibit a maximum at $\omega = 1.98/\tau$ where D_{it} is equal to $2.5(G_p/\omega)_{max}$ according to the conductance method.[17] Another way for extracting the D_{it} is to measure the C_m at fixed low- and high-frequency values. Such measurement provides high-frequency capacitance (C_{HF}) and low-frequency capacitance (C_{LF}) values, which are used in high–low frequency capacitance (C_{HF}-C_{LF}) method. The advantage of this method is that it is easier and requires less time when compared with the conductance method. The logic of this method is considerably simple; no D_{it} can respond to the high signal if the capacitance is measured at sufficiently high frequencies, whereas all traps will respond to the low signal if the capacitance is measured at sufficiently low frequencies. Thus, the voltage-dependent profile of D_{it} can be extracted from the difference of the two C-V curves of C_{HF} and C_{LF}.

Studies on $Ca_3Co_4Ga_{0.001}O_x$ interfacial layer and its effects on current–voltage characteristics suggest that this interfacial layer material is a promising material regarding the high rectification ratio and conformity to thermionic emission theory through Gaussian distribution of barrier height.[18,19] These studies basically are based on I-V characteristics. For frequency dependence of electrical parameters, C-V and G/ω-V characteristics need to be explored. Moreover, density and distribution of interface traps in structures that have $Ca_3Co_4Ga_{0.001}O_x$ as interfacial layer need to be investigated because D_{it} does not only cause small signal energy loss but also affects other device parameters and causes deviations. Therefore, Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/n-Si structures were fabricated in this study and later conductance and high–low frequency capacitance (C_{HF}-C_{LF}) methods were utilized for the extraction of D_{it} in order to achieve a better understanding of voltage-dependent profiles of D_{it} and τ of this MPS type structure. In addition, depletion capacitance data were utilized for the extraction of electrical parameters and obtained parameters' frequency dependence was reported as well.

EXPERIMENTAL

Sol–gel method was utilized for synthesizing the 2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$. First, using the relevant proportions, a mixture of metal compounds with acetate and nitrate and deionized water was prepared. Later, polyvinyl alcohol (PVA) polymer was included in this mixture so that it can be deposited on the semiconductor wafer. A mixture of graphene flakes and deionized water was prepared in an ultrasonic bath. Once graphene nanoparticles were dispersed in deionized water, the mixture was poured into the previously prepared polymeric solution. For the fabrication of Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/n-Si structures, a P-doped single-crystal n-Si with a resistivity of 0.001–0.005 Ω.cm, thickness of 250 μm, and crystal orientation of (100) was used. First, the wafer was cleaned with conventional chemicals in an ultrasonic bath and then rinsed in deionized water of 18 MΩ cm for a sufficient time and later it was dried using nitrogen gas. Highly pure (99.999%) Au was thermally evaporated on the entire back of the n-Si wafer at 10^{-6} Torr pressure in a thermal evaporation system by which the metal layer thickness and the deposition rates were monitored using a quartz crystal thickness monitor. After the deposition, a layer with 1500 Å thickness was deposited on the back side of the wafer. Then the wafer was annealed at 500 °C for about 5 min under a nitrogen atmosphere. Thus, the Au layer was sintered to exhibit ohmic back contact behavior. Before the deposition of rectifying contact, 2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$ layer was grown using electrospinning method. The solution was first taken into a syringe whose needle tip was kept 18 cm away from the metal collector on which the wafer was mounted so that fibers were deposited on the wafer. A potential difference of 17 kV was applied so that electrostatic force forms fibers out of the solution and sends them on the wafer. Later, rectifying contacts were deposited using highly pure (99.999%) Au via a shadow mask, which helps to form disk-shaped rectifying contacts with a diameter of 1 mm and thickness of 1500 Å. Later the wafer was pasted on Cu holder for measurements using Ag paste for the measurements. Capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements were held between −2 V and 6 V at room temperature using a computerized HP 4192A LF impedance analyzer (5 Hz to 13 MHz), which is connected to a computer through an IEEE-488 ac/dc converter card. During the measurements, the sample was kept in dark at room temperature and the frequency of a.c. signal was changed from 5 kHz to 500 kHz for each measurement.

RESULTS AND DISCUSSION

Figure 1 and its inset show G/ω-V and C-V plots, respectively, in the frequency range of 5 kHz and 500 kHz, respectively. It is seen in the figure that the structure exhibits typical voltage-dependent behavior of a MIS structure through inversion, depletion, and accumulation regions. The inset of Figure 1 exhibits dispersion with frequency. Furthermore, there exists peak behavior in a way that C-V curves fold back after reaching a maximum point. Such

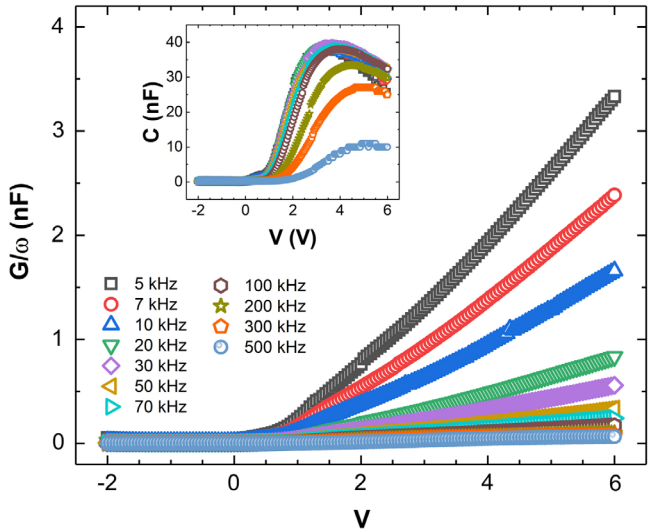

Figure 1. C-V plots of Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure. Inset shows G-V plots of the structure. [Color figure can be viewed at wileyonlinelibrary.com]

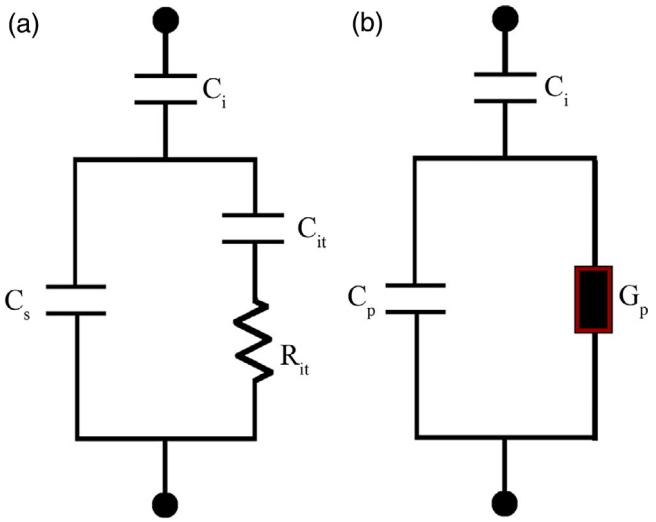

Figure 2. Equivalent circuit of Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure: (a) Low-frequency limit with contribution of interface traps and (b) representation with parallel capacitance and parallel conductance. [Color figure can be viewed at wileyonlinelibrary.com]

peak behavior in C-V curves is basically due to interface states and partly due to series resistance of the structure.[2,4,14] It is clear that this peak behavior loses intensity with increasing frequency and almost disappears at 500 kHz. It is also seen that C takes higher value when it is measured at 5 kHz. On the other hand, low-frequency measurement (5 kHz) yields lower G values compared to high-frequency measurement (500 kHz); however, it can be easily seen that G/ω, which is preferably used because it has same unit with C, would have larger values for low-frequency measurement. Such behavior of capacitance and conductance is partly due to the contribution of the trapped charges to total C and G/ω. If there were no traps, then the equivalent capacitance of the device is formed by insulating layer's capacitance in series connection with that of semiconductor. However, this case is approximated only at sufficiently high frequencies where traps cannot follow the a.c. signal. The equivalent circuit could be drawn as shown in Figure 2(a) if we cannot ignore the effect of D_{it}. In the figure, C_{it} and R_{it} are capacitance and resistance due to interface traps. Therefore, C-V and G-V plots exhibit dispersion with frequency because of the excess capacitance and conductance coming from the trapped charges. Nevertheless, it should be noted that such dispersion is not solely due to D_{it}, other factors such as series resistance of the structure also cause deviation from the ideal case.[20]

As mentioned earlier, one of the methods for extraction of D_{it} values is high–low frequency method that utilizes capacitance data. According to this method, D_{it} can be calculated using the following equation[21]:

$$D_{it} = \left(\frac{1}{qA}\right)\left\{\left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1}\right\} \quad (1)$$

where A is the area of rectifying contact, q is the elementary charge, C_i is the capacitance of insulating layer, and C_{LF} and C_{HF} are the capacitance values measured at low- and high-frequencies, respectively. Figure 3 shows voltage-dependent profile of D_{it}. This plot suggests that D_{it} is particularly effective at forward biases with minimum effect during inversion, also the peak in D_{it}-V curve is consistent with the C-V plots in terms of excess capacitance caused by D_{it}.

D_{it} values of the structure were also calculated using conductance method. As shown in Figure 2, equivalent circuit of the device [-Figure 2(a)] can be simplified into the one in Figure 2(b) where C_p and G_p are parallel capacitance and parallel conductance, respectively. For the extraction of D_{it} via conductance method, first, G_p/ω values were calculated using the following equation[17]:

$$\frac{G_p}{\omega} = \frac{\omega^2 G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2)$$

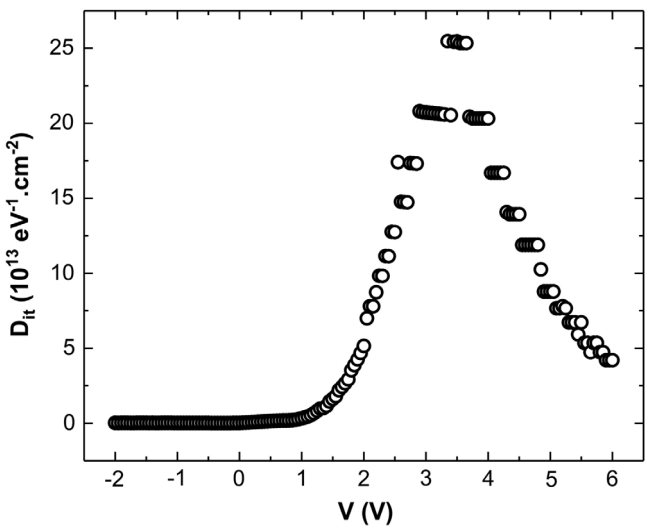

Figure 3. Voltage-dependent profile of interface traps in Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure via high–low frequency method.

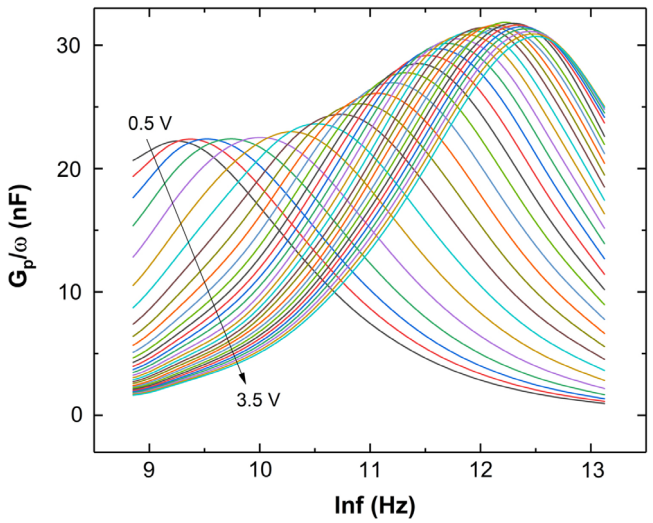

Figure 4. G_p/ω-lnf plots of interface traps of Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure. [Color figure can be viewed at wileyonlinelibrary.com]

Later G_p/ω-lnf plots were obtained with bias voltage steps of 0.05 V from 0.5 V to 3.5 V. However, G_p/ω-lnf plots were shown in Figure 4 with bias voltage steps of 0.1 V in order to make the figure clearer. Each G_p/ω-lnf curve has a local maximum, which is later utilized to extract lifetime of the traps. According to conductance method, G_p/ω is given by[17];

$$\frac{G_p}{\omega} = \frac{qAD_{it}}{2\omega\tau}\ln\left(1+(\omega\tau)^2\right) \quad (3)$$

Local maximum of G_p/ω-lnf requires that first derivate of G_p/ω is equal to zero, thus the value of $\omega\tau$ at the local maximum is equal to 1.98; therefore, τ can be calculated by dividing 1.98 with ω value that corresponds to the local maximum of G_p/ω-lnf plots. Using $\omega\tau = 1.98$, D_{it} is derived from eq.3 as in the following equation[17]:

$$D_{it} = \frac{(G_p/\omega)_{max}}{0.402qA} \quad (4)$$

where $(G_p/\omega)_{max}$ stands for the G_p/ω value at the local maximum of G_p/ω-lnf plots. Figure 5 shows bias voltage dependence of D_{it} and τ. It is seen that τ decreases with increasing bias voltage, which in turn makes it easy for trapped charges to follow the a.c. signal. This is consistent with the larger D_{it} values at higher bias values. D_{it} values of conductance method and high–low frequency method are approximately of the same order. Also, their bias voltage dependence looks quite similar that D_{it} becomes effective in the forward biases. However, it is clear that high–low frequency method yields larger D_{it} values. This discrepancy is mainly due to the usage of different methods. High–low frequency method basically performs integration of over interface traps that have different lifetime values. Therefore, D_{it} values obtained by high–low frequency method correspond to different kinds of interface traps. This suggests that there exits interface traps that conductance method fails to detect because these traps are too slow.[22] Obtained D_{it} values are on the order of 10^{13} eV^{-1} cm^{-2}; this value is reasonable for Schottky type structures with organic interfacial layer particularly considering some other PVA-based structures, which have D_{it} values above 10^{16} eV^{-1} cm^{-2}.[3,23]

Besides D_{it}, several other electrical parameters of the device were obtained as well. For this purpose, C^{-2}-V plots were drawn and the capacitance data of linear parts that correspond to depletion layer were utilized. For metal–semiconductor structures with interfacial insulator layer, depletion layer capacitance is given by[12];

$$C = \left[\frac{qA^2\varepsilon_s\varepsilon_o N_D}{2(V-V_o)}\right]^{\frac{1}{2}} \quad (5)$$

where ε_s is the dielectric constant of semiconductor, ε_o is the permittivity of vacuum, N_D is the doping concentration of donor atoms, and V_o is given by V_{bi}-kT/q such that V_{bi} is built-in or diffusion potential. Thus, slope and interception point of linear parts of C^{-2}-V plots can be utilized to calculate N_D and V_{bi}. Once these parameters are obtained, other electrical parameters can be calculated as well. Fermi energy (E_F) is calculated through the following equation[12]:

$$E_F = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \quad (6)$$

where N_C is the effective density of states in the conduction band of semiconductor, which is equal to 4.82×10^{15} $[T(m_e^*/m_o)]^{3/2}$. After the Fermi energy values are obtained, barrier height (Φ_B) of the structure can be calculated using the following equation[12]:

$$\Phi_B = V_{bi} + E_F - \Delta\Phi_B \quad (7)$$

Here, $\Delta\Phi_B$ is barrier lowering due to image forces and it is given by[12]:

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}} \quad (8)$$

where E_m is the maximum electric field, which is given by[12]

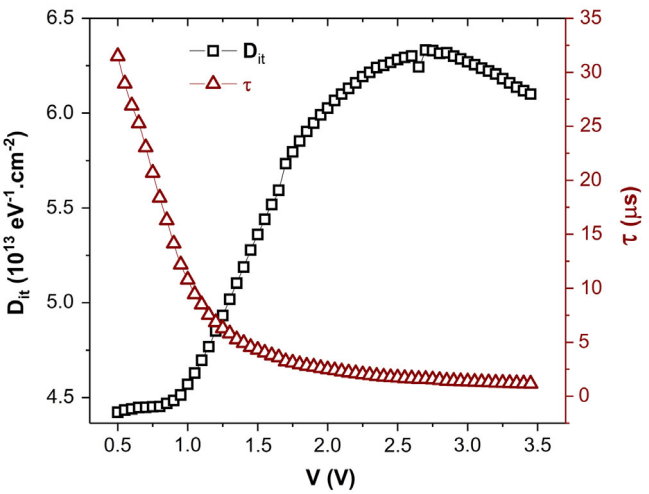

Figure 5. Voltage-dependent profile of interface traps and their lifetime in Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x$/*n*-Si structure via conductance method. [Color figure can be viewed at wileyonlinelibrary.com]

Table I. Frequency Dependence of Electrical Parameters of Au/2% GC-Doped $Ca_3Co_4Ga_{0.001}O_x/n$-Si Structure

f (Hz)	N_D (cm^{-3})	V_{bi} (eV)	W_D (cm)	E_F (eV)	$\Delta\Phi_B$ (meV)	Φ_B (eV)
5000	4.80×10^{13}	0.080	6.08×10^{-4}	0.316	3.638	0.393
7000	6.35×10^{13}	0.113	6.29×10^{-4}	0.309	4.257	0.418
10 000	6.57×10^{13}	0.138	6.82×10^{-4}	0.308	4.507	0.441
20 000	7.20×10^{13}	0.206	7.96×10^{-4}	0.306	5.101	0.507
30 000	8.72×10^{13}	0.287	8.54×10^{-4}	0.301	5.813	0.582
50 000	1.09×10^{14}	0.406	9.06×10^{-4}	0.298	6.704	0.694
70 000	1.16×10^{14}	0.488	9.63×10^{-4}	0.293	7.134	0.774
100 000	1.21×10^{14}	0.576	10.28×10^{-4}	0.292	7.502	0.861
200 000	1.52×10^{14}	0.874	11.29×10^{-4}	0.286	8.816	1.152
300 000	1.87×10^{14}	1.148	11.64×10^{-4}	0.281	9.951	1.419
500 000	2.91×10^{14}	1.845	11.85×10^{-4}	0.270	12.502	2.102

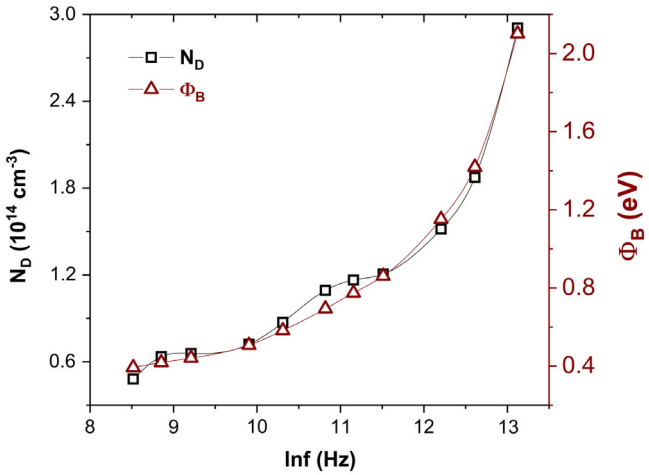

Figure 6. Frequency dependence of N_D and Φ_B of Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x/n$-Si structure. [Color figure can be viewed at wileyonlinelibrary.com]

$$E_m = \sqrt{\frac{2qN_D V_{bi}}{\varepsilon_s \varepsilon_o}} \quad (9)$$

Moreover, depletion layer width, W_D, of the structure was also obtained using C^{-2}-V data via the following equation[12]:

$$W_D = \sqrt{\frac{2\varepsilon_s \varepsilon_o V_{bi}}{qN_D}} \quad (10)$$

Table I shows the electrical parameters that are calculated using depletion layer capacitance approach. It was found that all parameters extracted from C^{-2}-V data are frequency dependent. The effect of increasing frequency on depletion layer width is such that the value of W_D is almost doubled in the studied frequency range. On the other hand, E_F became smaller with increasing frequency because N_D is a function of frequency. Figure 6 shows frequency dependence of N_D and Φ_B of the structure. It is seen that they both increase with increasing frequency and interestingly their dependence to frequency is quite similar such that almost overlapping curves were obtained for fixed y-axis scales.

CONCLUSIONS

In this study, Au/2% GC-doped $Ca_3Co_4Ga_{0.001}O_x/n$-Si structure was fabricated and its C-V and G/ω-V measurements were conducted between 5 kHz and 500 kHz to investigate its electrical parameters. Depletion layer capacitance was utilized to obtain electrical parameters of the structure. Obtained electrical parameters showed strong dependence on frequency of the signal in a way that N_D, W_D, and Φ_B increased, whereas E_F decreased with increasing frequency. Moreover, the frequency dispersion in C-V curves was associated with excess capacitance due to interface states. First, D_{it} was calculated using high–low frequency method and obtained D_{it}-V profile with peak behavior was consistent with the contribution of excess capacitance to C-V curves. Later, D_{it} and its lifetime values were extracted from G_p/ω-lnf plots, and it was found that this method also reveals a peak in the forward bias region corresponding to excess capacitance contribution observed in C-V curves. Different methods revealed different values for D_{it}, however they do not differ seriously that the order of 10^{13} $eV^{-1}.cm^{-2}$ was obtained for the studied structure with a decrease in lifetime of the states.

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