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The influence of the physicochemical processes on the electrical response of Al/p-Si structure with etched surface

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Abstract
In this paper, the electrochemical etching process is used for surface modification of the p-Si wafer, named as porous silicon (PS), in the metal–semiconductor (MS) type Schottky diode (SD) with a structure of Al/p-Si. Five regions of PS wafer with different etching rates are selected for comparison of them which are called P_2, P_3, P_4, and P_5 (P_1 is the reference area without porosity). The morphological, structural, and electrical properties of the PS used in the MS-type SD are investigated using field-emission scanning electron microscope (FE-SEM) images, energy dispersive X-ray (EDX) analysis, and current–voltage (I–V) characteristics, respectively. The FE-SEM images show a meaningful effect on the porosity. The EDX spectrum demonstrates the importance of the chemical effects in addition to the physical changes in the porosity process of the p-Si wafer. The reverse-saturation current (I_0), ideality factor (n), barrier height at zero-bias (Φ_{B0}), and series/shunt electrical resistances are also computed and compared. Some of these parameters (n, Rs, BH) are determined using different methods, namely Thermionic emission (TE), Cheung functions, and modified Norde, and they exhibit strong agreement with each other. The energy-dependent profiles of surface states (Nss) are estimated from the I–V data by considering the voltage dependence of Φ_B (V) and n(V). All the experimental findings indicate that the etching process of the p-Si wafer significantly influences the electrical performance of the Al/p-Si Schottky diode by increasing the extent of etching.

Keywords Shottky diode (SD) · Porous silicon surface · Electric properties · Energy dependent profile of surface states

1 Introduction

In recent years, the primary challenges in metal–semiconductor (MS) type contacts or Schottky diodes (SDs), whether with or without a native or grown interlayer, revolve around enhancing their performance. This involves reducing parameters such as Rs, Nss, leakage current, while simultaneously increasing the rectifying rate ($RR = I_F/I_R$ at sufficiently high forward and reverse bias voltages), shunt resistance (Rsh), and barrier height (BH). The structural characteristics and electrical properties of these devices typically rely on factors like surface preparation, the nature of the interlayer at the metal/semiconductor interface, BH, doping levels, operating frequency, applied voltage, and temperature [1–6]. Therefore, in the last five decades, especially semiconductor nanostructures have been considered much attention because of their physical and chemical properties to improve their performance [7–10]. Among these inorganic materials (Si, Ge, GaAs, InP, CdS/CdTe), Si is one of the oldest and has low-cost, high stability, but unwanted high leakage current and N_{ss}. Due to its unique properties, it is used in many applications in various fields, especially in electronics and semiconductor device fabrication technology, yet [11–14]. The unique characteristics of the Si are more evident when its dimensions are reduced. By deceasing the size and dimension of Si, its physical and chemical properties change due to the quantum confinement effect [15, 16].

Utilizing Si nanostructures instead of traditional antireflection (AR) layers presents a compelling alternative due to their unique light-trapping capabilities, particularly in the realm of photovoltaic devices. Si nanostructures have the

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potential to enhance light absorption over a broad spectrum range by exploiting various optical effects, such as light trapping, scattering, and resonance phenomena. Unlike conventional AR coatings that operate based on interference effects and are limited to specific wavelengths, Si nanostructures offer a more versatile and efficient means of managing light at the nanoscale. By leveraging the design flexibility and tunability of Si nanostructures, tailored optical properties can be achieved to maximize light absorption in photovoltaic applications, thereby improving overall device performance and efficiency [17–20].

There are various methods used for the manipulation of Si nanostructures to change its physical properties such as doping by other materials [21, 22] which is thermal annealing [23, 24], plasma treatment [25, 26], and electrochemical etching [8, 9]. The preparation of Si nanostructures, including Silicon Nanowires (SiNWs) and Silicon Nanorods (SiNRs) on the surface of silicon, has captured the interest of scientists. These nanostructures exhibit unique properties and have shown great potential for various applications in nanotechnology and electronics [27–30]. One of these types of manipulations is to create porosity in the Si structure and the production of PS. PS is a dielectric material composed of silicon dioxide (SiO_2) and air, which has a structural heterogeneity much smaller than normal light wavelength [31]. Among these methods, electrochemical etching is one of the most widely used methods for the surface treatment of Si wafers. In this method, the surface morphology of the samples has changed with the condition of the electrochemical etching [32]. The surface treatment contains the formation of porosity in the structures of the Si semiconductors have different applications such as nonlinear optics [33], biology [34], solar cells (SCs) [35], fabrication of Bragg-reflectors [36], microelectronics [37], waveguides [38], optical filter [39], gas sensors [40], photoluminescence devices in the visible region [41], energy [42], drug industry [43], biotechnology [44], and some other complex optical devices due to its high surface-to-volume ratio, high reactivity, luminescence properties at room temperature, and its adaptive nature [45]. There are several studies on the optical and structural applications of PS reported by researchers [46–48].

Furthermore, the electrical characteristics and energy-dependent interface states of Schottky diodes (SDs), whether with or without an interlayer, have received substantial attention due to their significance in technological applications. An increase in the dielectric constant leads to a higher capacity for storing electronic charges or energy, resulting in the reduction of numerous factors such as N_{ss}, R_s, and dislocations [14, 15]. Consequently, recent research efforts have focused on manipulating the modification of electronic and transport properties in conventional MS-type SDs by incorporating various interlayers with high-dielectric materials. This approach aims to mitigate leakage current, ideality factor (n), N_{ss}, and series resistance (R_s), ultimately enhancing the device's overall performance [49–52]. To our knowledge, the study of the electrophysical properties of PS structures has not been seriously investigated in detail and so nonclarified yet. In this research, we aimed that are conducted to control the main electrophysical parameters of the Al/p-Si (MS) structures by modifying the surface morphology of p-Si using the etching process. For this aim, the p-Si surface is divided into 5 partition with various porosity P_1 to P_5 areas. The surface morphology and structural analysis are investigated by recording the FE-SEM images and EDX spectrum, respectively. Moreover, the *I–V* measurements are performed in a wide voltage range (± 1.5 V). The main electronic features of the MS-type SD with a structure of Al/p-Si that its semiconductor has been poroused are calculated by the TE, Cheung functions, and modified Norde techniques. The energy-dependent N_{ss} profile are obtained at P_2, P_3, P_4, and P_5 with different degree of porosity. The influence of the electrophysical etching process of the p-Si wafer on the electric response of Al/p-Si SD will be thoroughly discussed.

2 Experimental details

2.1 Materials, preparation, and instruments

A p-type double-side polished (100)-oriented p-Si wafers with a specific resistivity of 1–10 Ω cm were used to prepare porous silicon. The Si substrate was utilized along with a 50% HF solution, distilled water, and 99.99% ethanol. The process involved the electrochemical etching of silicon in the HF solution, leading to the partial dissolution of Si. It is vital to investigate and comprehend the influence of various factors that govern this process. The choice of electrolyte is crucial in the formation of porous silicon, with HF typically used in concentrations up to 50% in distilled water. After rinsing the samples with ethanol to eliminate any dirt, they were immersed in a diluted (50%) Hydrofluoric acid (HF) solution for 15 min to remove any native oxide layer. Subsequently, the samples were rinsed with ethanol again and left to dry in the ambient atmosphere for a few minutes. They were then stored immersed in plastic containers filled with methanol to prevent the reformation of oxide layers on their surfaces. Each sample was placed at the bottom of a Teflon singlet anodizing system and secured by a support material sheet, acting as the Anode, while a platinum mesh rod was positioned perpendicular to the Si surface at a distance of 1 cm, serving as the cathode. HF circulation during the etching process contributes to achieving good depth uniformity and enhances safety. A lateral geometry approach for porous silicon formation has been proposed, where a contact is deposited on the surface where the porous silicon will be formed. This method promotes lateral rather than depth-wise

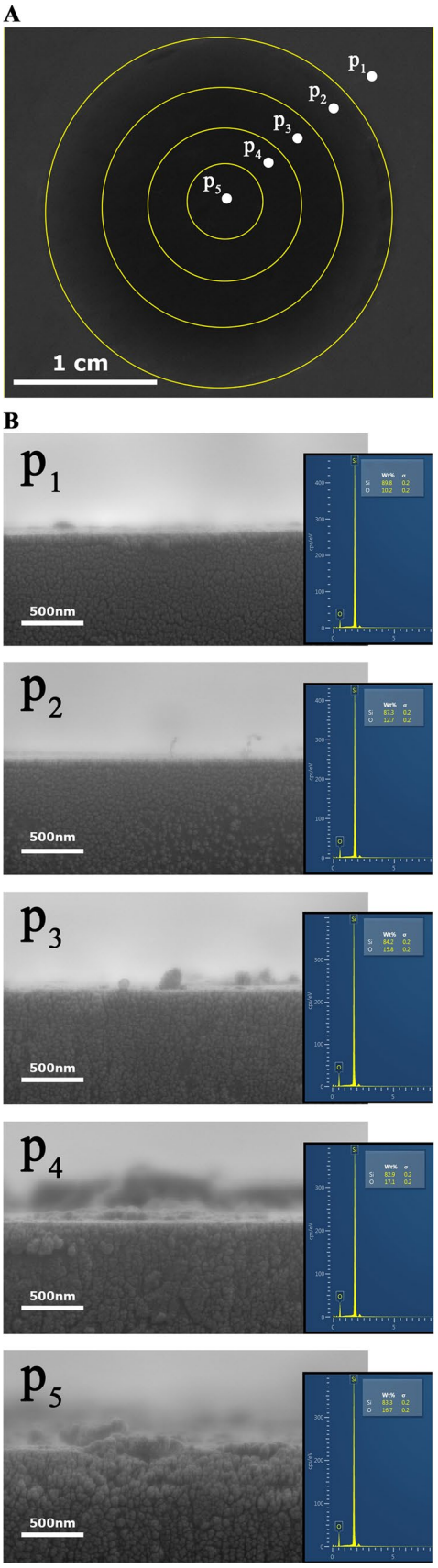

Fig. 1 The schematic image of different porous silicon regions, FE-SEM images and EDX graphs of different points of the electrochemically etched p-Si (P_1 to P_5)

porous silicon formation, resulting in flat porous silicon/Si interfaces. Understanding the various factors influencing the electrochemical etching process is essential for producing uniform and high-quality porous silicon layers with desirable properties for diverse applications.

The prepared porous Si was utilized as an MS-type Schottky diode (SD) without any initial contact. To evaluate the surface morphology of the treated p-Si wafer, FE-SEM analysis was performed using the TeScan-Mira III instrument from Czech Republic. Electrical measurements were conducted on the sample using the Keithley 2450 Sourcemeter I–V characteristics system from the USA, spanning a broad range of applied bias voltages (± 1.5 V) at room temperature.

2.2 FE-SEM and EDX analysis

Figure 1 presents a schematic depiction of distinct porous silicon regions, illustrating their connection to FE-SEM images of porous silicon (PS) with varying degrees of p-Si surface etching, along with their corresponding EDX spectra. In this figure, the area P_1 is related to the normal silicon region without manipulation, and the areas P_2 to P_5 correspond to the regions of the least to the highest amount of the etching process performed on the surface of the p-Si wafer, respectively.

As seen from Fig. 1, by increasing the amount of etching process, the porosity increase, so that the average value of porosity size has changed from 300 nm for the least amount of etching (P_2) up to 2 µm for the maximum amount of etching (P_5). The mean size of a different region of silicon is introduced in Table 1.

It is obvious that the oxygen species is the second sharp peak in the EDX spectrum after the Si peak. It indicates that the porosity process has a significant chemical effect in addition to the physical changes of the p-Si surface.

3 Results and discussion

The semi-logarithmic forward and reverse bias *I–V* characteristics of the different regions (P_2–P_5) of a p-type silicon wafer are shown in Fig. 2a.

The essential electrical characteristics, including I_0, n, Φ_{B0}, R_s, and R_{sh} of the manufactured MS-type Schottky diode (SD), are derived from the forward and reverse bias current–voltage (*I–V*) measurements using conventional thermionic emission (TE) theory. The expression describing

Table 1 Average porosity values at different regions

Region	P_2	P_3	P_4	P_5
Size (nm)	300	700	1500	2000

the forward bias *I–V* relationship in terms of TE theory for $V \geq 3kT/q$ is provided as follows [53, 54]:

$$I = AA^{*}\exp\left(-\frac{q\Phi_{B0}}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right]. \quad (1)$$

The terms before the square brackets are the I_0 quantity which is obtained from the linear part of Ln(*I*)–*V* plot, A^* is the effective Richardson constant, and other terms in Eq. 1 are well-known parameters of the MS-type SD explained elsewhere [53, 54]. The values of I_0 for the P_2, P_3, P_4, and P_5 regions were found as 99.8 nA, 62.3 nA, 13.4 nA, and 15.2 nA, respectively. The n value is determined as the reciprocal of the slope derived from the linear portion of the natural logarithm of the current (*I*) versus voltage (*V*) plot, as illustrated below [53]:

$$n = \frac{q}{kT}\left[\frac{d(V-IR_s)}{d(lnI)}\right]. \quad (2)$$

Hence, the value of Φ_{B0} can be computed by utilizing the determined values of I_0 and the surface area (*A*) of the Schottky diode (SD), as shown by [54]:

$$\Phi_{B0} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_0}\right). \quad (3)$$

As shown in Fig. 2a, the P_1 region without the etching process has almost an ohmic behavior, and gradually, by increasing the amount of the etching process, the I–V plot of the P_2 to P_5 regions exhibits rectifier behavior and these plots have a good linear region in the large bias voltage at intermediate bias region. The least rectifier rate ($RR = I_F/I_R$ at ± 1.5 V) was found as 25.5 for the P_2 region with the least porosity, and the highest RR was found to be 47.2 for P_4 and its amount is 9.7 related to P_5 region. In addition, the values of n were computed as 2.6, 2.5, 2.4, and 2.7 for the P_2, P_3, P_4, and P_5 regions, respectively. The values of n for each porous region are higher than the ideal case ($n = 1$), indicating that it deviates from standard thermionic emission (TE) theory. These higher values of n are attributed to the existence of a native SiO_2 insulator layer, barrier height inhomogeneity at the MS junction, and N_{ss} at the Al/p-Si interface [5, 49].

The series resistance (R_s) in Schottky diodes typically arises from various factors, including the formation of rectifying/ohmic contacts on the semiconductor, the bulk resistance of the semiconductor material, the contact points established by the probe wires connected to the Schottky contact, and dislocations occurring within the semiconductor's bandgap. However, the actual values of R_s and R_{sh} are representative of sufficiently high forward and reverse biases, respectively. Different methodologies are employed to quantify R_s, each associated with distinct voltage regimes. Consequently, R_s is calculated using Ohm's law, Cheung, and Norde techniques, and the results are compared. As a result, the values of I_0, n, Φ_{B0}, R_s, R_{sh}, and RR for various regions of porous silicon (PS) are presented in Table 2 for reference.

As shown in Table 2, P4 has the least n and I_0, and the highest R_s, R_{sh}, RR, and Φ_{B0}. Therefore, increasing the etching process (up to the P_4 region) improves the quality of the MS-type SD and after that, the performance of the MS-type SD decreased with increasing porosity. Both R_s and R_{sh} values increase by increasing porosity. Increasing the R_{sh} value reduces and enhances the leakage current and the rectifying ratio of the MS-type SD. As shown in Table 2, the higher values of n and R_s indicate the deviation of ideal case or

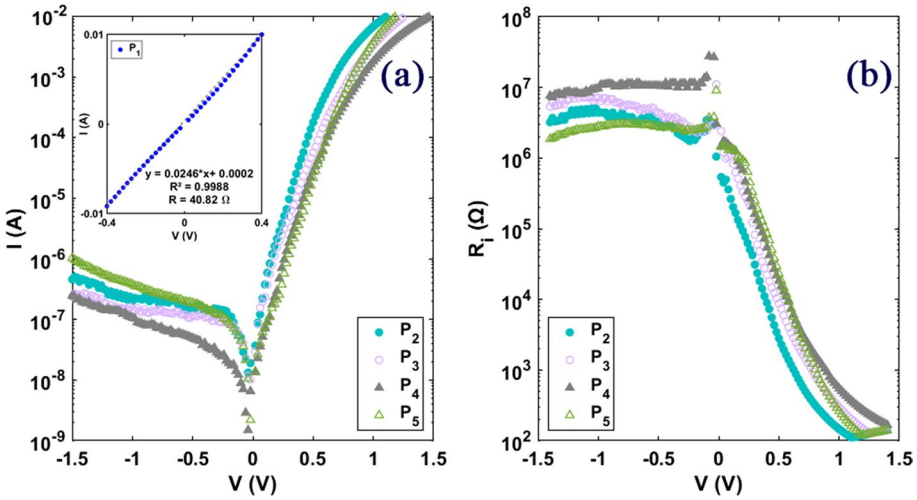

Fig. 2 The semi-logarithmic of **a** I–V and **b** R_i–V plots related to a different region of PS (P_2 to P_5)

Table 2 Main electrical parameters for different regions of PS at room temperature

Regions	I_0 (nA)	n	Φ_{B0} (eV)	RR	R_s (Ω)	R_{sh} (MΩ)
P_2	99.8	2.6	0.71	25.5	111	3.36
P_3	62.3	2.5	0.72	41.9	202	5.60
P_4	13.4	2.4	0.76	47.2	370	8.06
P_5	15.2	2.7	0.76	9.7	162	2.07

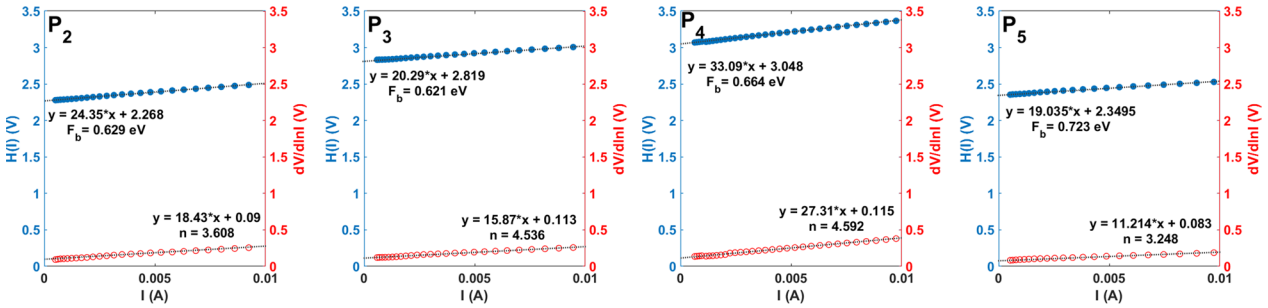

Fig. 3 The plots of dV/dln(I) and H(I) vs I at different regions of PS (P_2 to P_5)

standard TE theory due to the formation of many N_{ss} and inhomogeneity of BH at the MS junction [55–60].

As per the models established by Cheung [59], the series resistance (R_s) can be determined using the equations provided, based on the sufficiently high forward bias I–V data [59]:

$$\frac{dV}{dln(I)} = n\left(\frac{kT}{q}\right) + IR_s, \tag{4a}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_{B0}. \tag{4b}$$

In Eqs. 4a and 4b, the parameter IR_s represents the voltage drop across the series resistance (R_s) in the MS-type SD. The expressions for dV/dln(I) and H(I) are derived from the I–V characteristics data. The experimental plots depicting dV/dln(I) and H(I) as functions of current (I) for various porous silicon (PS) regions are presented in Fig. 3.

Upon fitting the curve to a linear model and employing Eq. 4a, both R_s and n can be determined from the slope and the intercept of the fitted line. Likewise, the second Cheung function is employed to compute R_s and Φ_{B0} values, extracting them from the slope and intercept of H(I)–I plots.

Additionally, the R_s and Φ_{B0} values are able to be computed using Norde method developed by Bohlin for higher value of n as [47]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right). \tag{5}$$

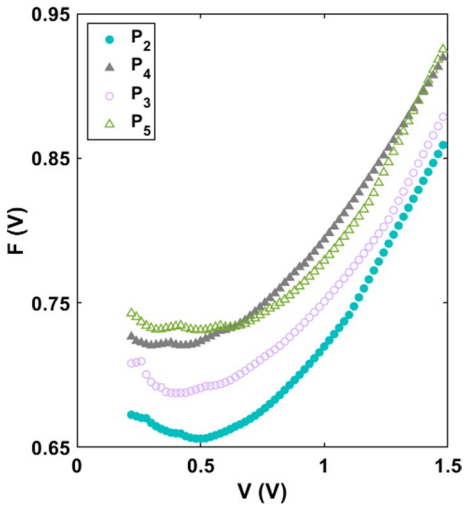

Fig. 4 The plots of F(V) vs V for different regions of PS (P_2 to P_5)

In Eq. 5, γ represents a dimensionless integer that should be chosen to be greater than n. Following this approach, R_s and Φ_B values can be determined by utilizing the minimum value of the F(V) function (refer to Fig. 4) and the corresponding voltage and current values. This is achieved by applying the following relationships [47]:

$$R_s = \frac{kT}{q}\frac{\gamma - n}{I_{min}}, \tag{6}$$

$$\Phi_{B0} = F\left(V_{min}\right) + \frac{V_{min}}{\gamma} - \frac{kT}{q}. \tag{7}$$

Table 3 Some electrical parameters extracted from the different methods for regions of P_2 to P_5

Regions	n		R_s (Ω)				Φ_B (eV)		
	TE	dV/dln(I)	TE	Norde	dV/dln(I)	H(I)	TE	Norde	H(I)
P_2	2.6	3.6	111	117	17.9	24.2	0.69	0.72	0.65
P_3	2.5	4.4	202	166	15.8	22.3	0.70	0.75	0.63
P_4	2.4	4.0	370	118	28.6	44.9	0.74	0.78	0.63
P_5	2.7	3.4	162	37.7	11.2	20.3	0.73	0.75	0.69

Consequently, the results for R_s, n, and Φ_B acquired through the utilization of Cheung's and Norde's methods are presented in Table 3. As demonstrated in Table 3, the calculated values of BH obtained from the Norde and Cheung techniques exhibit a strong agreement, whereas the R_s values do not align due to the different voltage regions employed. Notably, unlike the Norde method, the Cheung function is exclusively applied to the concave portion of the forward bias *I–V* curve [61–63].

The formation of N_{ss} during fabrication and the order in the periodic lattice also have remarkable influence on the performance of the SDs like R_s. Energy dependence of them can be calculate from the *I–V* data using following relations given by Roderick [54]:

$$n(V) = \frac{q}{kT}\frac{V_i}{I_i/I_0}, \tag{8a}$$

$$\Phi_e - \Phi_{B0} = \left(1 - \frac{1}{n(V)}\right)V. \tag{8b}$$

Moreover, the energy dependence of N_{ss} with respect to the bottom of the valance (E_V) at the surface of p-Si wafer is given as [54]:

$$E_{ss} - E_v = q(\Phi_e - V). \tag{9a}$$

Thus, the N_{ss} in terms of ($E_V - E_{ss}$) for p-type semiconductor can obtained as follow [13]:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right]. \tag{9b}$$

In this context, δ represents the interlayer thickness, W_D denotes the width of the depletion layer, $\varepsilon_i = 3.8\varepsilon_0$ stands for the permittivity of SiO_2, $\varepsilon_s = 11.8\ \varepsilon_0$ signifies the permittivity of silicon, and ε_0 represents the permittivity of vacuum. Thus, N_{ss} vs ($E_{ss} - E_v$) profile at different regions of PS are obtained using Eqs. 8a–9b and introduced in Fig. 5.

As shown in Fig. 5, the energy values of the N_{ss} at P_2, P_3, P_4, and P_5 regions are in the range of 0.42 eV − E_v to 0.67 eV − E_v. The magnitude of N_{ss} at 0.42 eV − E_v are 1.8×10^{13} eV^{-1} cm^{-2}, 2.7×10^{13} eV^{-1} cm^{-2}, 3.1×10^{13} eV^{-1} cm^{-2}, and 3.6×10^{13} eV^{-1} cm^{-2}, and

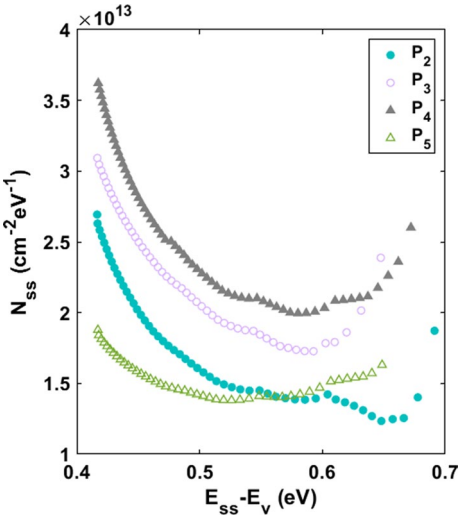

Fig. 5 The N_{ss} vs ($E_{ss} - E_v$) plots for different regions of PS (P_2 to P_5)

its value at 0.67 eV − E_v are 8.6×10^{12} eV^{-1} cm^{-2}, 9.9×10^{12} eV^{-1} cm^{-2}, 1.6×10^{13} eV^{-1} cm^{-2}, and 1.9×10^{13} eV^{-1} cm^{-2} at P_2, P_3, P_4 and P_5 regions of PS, respectively. Since the interlayer is inherently identical across all regions, the N_{ss} magnitude remains approximately consistent throughout. But the energy dependence of the N_{ss} at different regions is different. At low porosity region (P_2), the density of interface states decreased with increasing energy, while in high porosity region (P_5), with increasing energy, the N_{ss} decreased and then increased again after a minimum value.

4 Conclusions

The effect of etching process on the morphological, structural, and electrical features of the porous p-Si (PS) used in the MS-type SD was investigated using *I–V* measurement in the voltage range of ± 1.5 V at room temperature. For this aim, five regions of PS wafer with different etching rate were selected for comparison of them which are called P_1, P_2, P_3, P_4 and P_5. Firstly, surface morphology was investigated by FE-SEM images and experimental results show meaningful effect on the porosity. Moreover, the sharpened peak after

the Si peak in the EDX spectrum was related to the oxygen, indicating that the chemical effects are as crucial as physical changes in the porosity process on the p-Si surface. Secondly, the key electrical parameters, including I_0, n, Φ_{B0}, R_s, and R_{sh}, were computed and juxtaposed using standard TE (thermionic emission) theory, Cheung functions, and modified Norde functions, each pertaining to distinct voltage ranges. The energy-dependent profiles of interface states (N_{ss}) were likewise derived from forward bias *I–V* data, taking into account the voltage-dependent variations of $\Phi_B(V)$ and $n(V)$. All the results obtained collectively indicate that the electrophysical etching process of the p-Si wafer within the context of the MS-type Schottky diode (SD) significantly influences its electrical performance by amplifying the extent of the etching process.

Author contributions Yosef Badali: conceptualization, methodology, writing, reviewing and editing, data analyzing, Yashar Azizian-Kalandaragh: reviewing, methodology, writing, reviewing and editing, data analyzing.

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Data availability The data that support the findings of this study are available from the corresponding author, [Y-B], upon reasonable request.

Declarations

Conflict of interest The authors declare no financial or commercial conflict of interest.

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