J Mater Sci: Mater Electron (2024) 35:228

Thermal dependence on electrical characteristics of Au/(PVC:Sm_2O_3)/n-Si structure

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Received: 8 September 2023
Accepted: 25 December 2023

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ABSTRACT

In this study, we investigated the current–voltage (*I–V*) characteristics of Au/n-Si structure with an interfacial layer of Samarium Oxide (Sm_2O_3) nanoparticles (NPs) in polyvinyl chloride (PVC) matrix within a temperature range of 80–320 K. Applying the thermionic emission (TE) theory, essential electrical parameters such as reverse saturation current (I_0), ideality factor (n), zero bias barrier height (Φ_{B0}), series resistance (R_s), and rectification rate (RR) were carefully derived from the *I–V* data. The mean values of BH and Richardson constant obtained from the modified Richardson plot were determined to be 0.730 eV and 111.4 A/(cmK)^2, respectively. Remarkably, this A^* value closely matches its theoretical counterpart for n-type Si. Thus, our findings successfully highlight the effectiveness of the thermionic emission (TE) mechanism with the Gaussian distribution of BHs in explaining the *I-V-T* characteristics of the fabricated Schottky structure, shedding light on the intricate interplay between temperature and diode behavior. These insights offer valuable guidance for designing and optimizing thermal-sensitive devices based on this innovative structure.

1 Introduction

Schottky type structures with a polymer or oxide interfacial layer known as metal-polymer-semiconductor (MPS) or metal–oxide–semiconductor (MOS) show rectification feature due to the creation barrier between metal and semiconductor interface and the nature or magnitude of this barrier (*BH*) is usually dependent on selected work-function metal (Φ_m) and semiconductor (Φ_s) [1–3]. Furthermore, their efficacy and quality depend on various influencing factors, including the nature of the interface, the thickness and uniformity of the interfacial layer, the homogeneity of the barrier height (*BH*) at the metal/semiconductor (MS) interface, and the presence of interface traps between the metal and semiconductor materials [4–6]. Consequently, comprehending both potential current transport mechanisms and the characteristics of the barrier height, particularly at lower temperatures, becomes of paramount importance. Numerous mechanisms for current transport, including thermionic emission, thermionic-field emission, and field emission (TE, TFE, FE), as well as tunneling via interface traps or dislocations, generation recombination, and specialized distributions of barrier heights, contribute to carrier transition. It is

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https://doi.org/10.1007/s10854-023-11898-2
Published online: 25 January 2024

notable that certain mechanisms may dominate across specific temperature and voltage ranges [7–11].

Typically, *I–V* measurements are conducted either at a single temperature or within a limited temperature range, frequently encompassing room temperature or higher. This method inherently limits the depth of understanding regarding potential current transport (CT) mechanisms and the composition of the barrier height (BH) at the metal–semiconductor interface. Nevertheless, when these measurements are extended across an extensive spectrum of temperatures and bias voltages, they have the capacity to furnish substantial data, facilitating the identification of potential CT mechanisms and the inherent characteristics of the *BH* [12, 13]. Therefore, improving the quality and performance of the MS and metal/insulator/semiconductor (MIS) structures while lowering the production costs, surface states, series resistance, and leakage current is the primary technological and scientific challenge. However, the investigation of the CT mechanisms of these structures based on TE theory typically reveals a decrease in n and a rise in BH with rising temperature. When compared to its theoretical value, the Richardson plot, especially at low temperatures, deviates from linearity and provides a relatively low value for the Richardson constant (A^*) [14, 15].

In recent times, there has been significant interest in the utilization of organic polymers such as polyvinyl alcohol (PVA), polyvinylpyrrolidone (PVP), or Polyvinyl Chloride (PVC), as interfacial layers in the development of MIS Schottky structures, notably in electronic and optoelectronic applications [16–18]. It is believed that incorporating an appropriate metal component-doped organic polymer, between the metal and semiconductor can enhance the electrical characteristics and optical properties of Schottky Barrier Diodes (SBDs) [19–21]. The application of organic materials of this nature can also decrease leakage current, prevent reactions and inter-diffusion at the M/S interface, passivate unsaturated bonds on the semiconductor surface, and decrease the density of surface states (Nss) or dislocations. [22]. In a comparative analysis, Altındal et al. [20] manufactured semiconductor devices of Al/n-Si (MS), Al/PVC/n-Si, and Al/(PVC:Sm_2O_3)/n-Si (MPS) on the same Si-wafer, employing uniform conditions. They explored key parameters, including shunt resistance (R_{sh}), ideality factor (n), N_{ss}, and leakage current. Their findings revealed that, at room temperature, the relative rectification (*RR*) of the Al/(PVC:Sm_2O_3)/n-Si (MPS) structure exceeded that of the MS configuration by a factor of 117, while the N_{ss} value decreased for the MPS sample. Furthermore, in another study conducted by the same research group, the dielectric properties of the Al/(PVC:Sm_2O_3)/n-Si structure were examined, demonstrating excellent dielectric characteristics attributed to the incorporation of a polymer-based interfacial layer between the metal and semiconductor [21]. These outcomes underscore the feasibility of utilizing metal-doped polymers as interfacial layers at the MS interface, owing to their cost-effectiveness, flexibility, and ease of production in comparison to traditional insulator layers.

In this work, our primary aim was to comprehensively examine the fundamental electrical parameters and charge transport mechanisms of the Au/n-Si structure with an interfacial layer of Samarium Oxide (Sm_2O_3) nanoparticles (NPs) in a PVC matrix (PVC:Sm_2O_3) over a broad temperature range (80-320 K) to attain precise and dependable insights. We achieved this objective by analyzing the current–voltage-temperature (*I–V–T*) characteristics of Au/(PVC:Sm_2O_3)/n-Si semiconductor devices. Our experimental *I–V–T* analyses indicated that the charge transport mechanism can be effectively elucidated using the thermoelectric theory involving generation-recombination centers, even at elevated temperatures, rather than relying on conventional tunneling mechanisms such as field and thermionic-field emission.

2 Experimental details

Au/n-Si structure with (PVC:Sm_2O_3) interfacial layer were fabricated on a < 100 > -oriented single crystal n-silicon wafer measuring 300 μm in thickness and exhibiting a resistance range of 1–10 Ω·cm. First, for the cleaning process, the silicon wafer underwent etching in a heated solution comprising H_2O, NH_4OH, and H_2O_2 (in a ratio of 65:13:13 v/v). Subsequently, it was rinsed once more in deionized water (DIW) with a resistivity of 18 MΩ·cm. In the final step, the n-Si wafer was etched in a solution of H_2O: HF (in a ratio of 24:1 v/v) and underwent a subsequent wash with DIW. Subsequently, the wafer was dried in a nitrogen environment. To establish low-resistivity ohmic contacts, a 300 nm thick layer of Au (99.999%) was thermally evaporated onto the entire backside of the wafer at a vacuum pressure of 1.3×10^{-4} Pa. This Au layer was then annealed at 550 °C in a nitrogen atmosphere for a duration of 5 min. The (PVC:Sm_2O_3) interlayer was

grown onto the wafer as a subsequent step. Finally, pure Au was deposited onto the (PVC:Sm_2O_3) film in a circular shape, covering an area of 0.00785 cm^2, with a thickness of 150 nm to form Schottky contacts. For further details regarding the fabrication process of the polymer interlayer, as well as information regarding X-ray diffraction (XRD), field emission scanning electron microscopy (FE-SEM), energy-dispersive X-ray spectroscopy (EDX), UV–Vis spectroscopy, the schematic diagram of the MPS diode, and its energy-band diagram, please refer to our previous publications [20] and [21]. The *I–V* measurements were conducted using a Keithley-2400 source meter. The sample temperature was controlled using the Janis VPF-475 cryostat under a vacuum of 1.8×10^{-2} Pa and Lake Shore temperature control systems. These systems were integrated with a microcomputer linked to an IEEE-488 AC/DC converter card. The attainment of low temperatures, reaching as low as 80 K, was facilitated using liquid nitrogen within the Cryostat.

3 Experimental results

The current–voltage (*I–V*) characteristics of Au/(PVC:Sm_2O_3)/n-Si structure were investigated in a temperature range of 80 K to 320 K. The resultant findings are illustrated in Fig. 1(a) and (b), corresponding to the lower temperature (80–180 K) and the moderate temperature (200–320 K) ranges, respectively. The semi-logarithmic *I–V* plots distinctly reveal rectifying behavior, wherein the current magnitude escalates with increasing temperature. This behavior can be attributed to the reduction in the bandgap of silicon (Si) and the heightened thermal energy of charge carriers, as depicted in these figures. In simpler terms, it can be inferred that the Au/(PVC:Sm_2O_3)/n-Si structure exhibits an exceptionally strong sensitivity to temperature under various applied bias voltages or current conditions, similar to a temperature sensor. Furthermore, when investigating the semi-logarithmic *I–V* curves, a linear region is observed under forward bias conditions; however, this linearity deviates at higher forward bias voltages. This deviation stems from the influence of series resistance (R_s) and the effects of the interfacial organic layer. In cases where the semiconductor device encompasses an interfacial

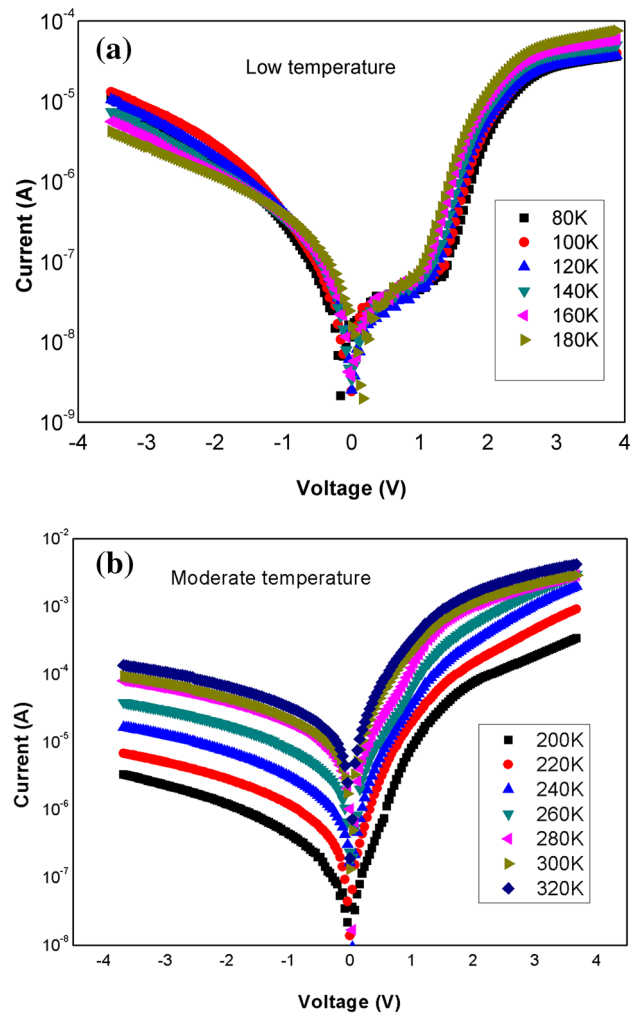

Fig. 1 The semi-logarithmic *I–V* curves of the Au/(PVC:Sm_2O_3)/n-Si, analyzed at **a** 80–180 K and **b** 200–320 K

insulating or organic layer, the applied bias voltage ($V_a = V_d + IR_s + V_i$) undergoes distribution among the depletion layer, R_s, and the interlayer.

To determine the basic electrical characteristics and current transport mechanisms of semiconductor devices belonging to the MS or MPS types and to detect any deviations from the conventional thermionic emission (TE) theory, we undertake an examination of the linear correlation between current and applied bias voltage. As per this theory, in instances where the diode incorporates a series resistance (R_s) and exhibits an ideality factor surpassing unity, the linear relationship remains valid under the condition of $qV \geq 3kT$ [1–4].

$$I = AA^{*}T^{2}\exp(-\frac{q}{kT}\Phi_{Bo})\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] = I_0[exp(q(V-IR_s)/nkT)-1] \quad (1)$$

The terms A, A^*, k, Φ_{B0}, T, and I_0 in Eq. 1 stands for the contact area, Richardson constant, Boltzmann constant, zero-bias BH, temperature in Kelvin, and reverse-saturation current, respectively. The second part of Eq. 1 can be ignored compared to the first part, and so the *I-V* relation for the linear part at the forward bias region can be given as follows [1–4]:

$$\ln(I) = \ln(I_0) + (q/nkT).V = \ln(I_0) + \tan((\theta)V \quad (2)$$

$\tan((\theta) = d\ln(I)/dV$ in Eq. 2 represents the slope linear portion of the ln(*I*)-*V* plot. At each temperature point, the intersection points and gradient of the linear segment within the ln*I* vs. *V* plot were employed to ascertain the respective values of I_0 and n. Subsequently, leveraging the value of I_0, we calculated the value of Φ_{B0} as depicted below [1–4].

$$\Phi_{Bo} = \frac{kT}{q}Ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \quad (3)$$

Table 1 contains the experimentally determined values of I_0, n, and Φ_{B0} at each temperature. Additionally, Fig. 2 provided both the value of n and the relationship between Φ_{B0} and temperature.

The electrical characteristics of I_0, n, and Φ_{B0} were determined as 7.60×10^{-12} A, 21.5, and 0.236 eV at 80 K, and 1.90×10^{-5} A, 7.17, and 0.615 eV at 320 K, respectively [Table 1]. These parameters strongly depend on temperature. As depicted in Fig. 2, the ideality factor (n) decreases with increasing temperature, while the barrier height (Φ_{B0}) increases. Notably, even at ambient temperatures, its value significantly exceeds unity. It is important to mention that this increase in barrier height does not conform to the negative temperature coefficient of the forbidden

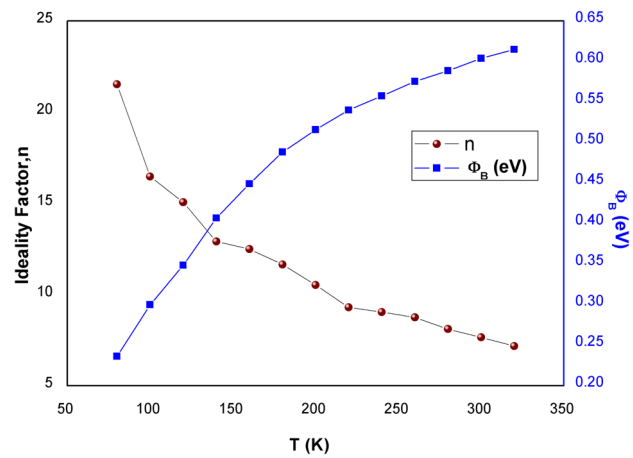

Fig. 2 The Φ_{B0} and n versus T curves of Au/(PVC:Sm_2O_3)/n-Si structure

Table 1 The temperature-dependence electrical characteristics of I_0 (A), n, Φ_{B0} (eV) and R_s (Ω) of the Au/(PVC: Sm_2O_3)/n-Si structure using TE theory

T (K)	n	I_0 (A)	Φ_{B0} (eV)	Rs (kΩ)
80	21.53	7.62×10^{-12}	0.236	106
100	16.47	7.10×10^{-12}	0.299	96.4
120	15.06	3.00×10^{-11}	0.349	104
140	12.91	4.04×10^{-11}	0.407	76.9
160	12.49	1.66×10^{-10}	0.449	65.3
180	11.65	6.25×10^{-10}	0.488	49.9
200	10.52	3.50×10^{-09}	0.516	9.06
220	9.30	1.60×10^{-08}	0.543	3.40
240	9.04	1.07×10^{-07}	0.556	1.50
260	8.75	4.50×10^{-07}	0.574	1.10
280	8.11	1.90×10^{-06}	0.587	1.20
300	7.65	5.50×10^{-06}	0.605	1.20
320	7.17	1.90×10^{-05}	0.615	0.80

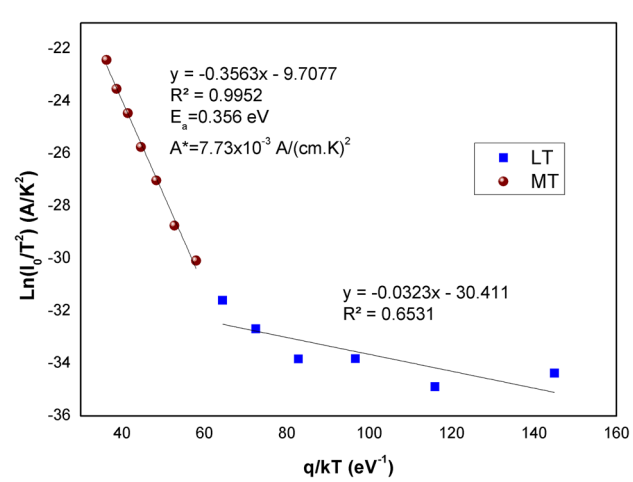

Fig. 3 $\ln(I_0/T^2)$ vs. q/kT curves of the Au/(PVC:Sm_2O_3)/n-Si structure

bandgap of semiconductors (e.g., -0.473 meV/K for Si).

In contrast, for the ideal semiconductor diode ($\alpha = dE_g/dT$), the change in barrier height, as determined from the forward bias *I-V* data, aligns with the negative temperature coefficient of E_g or *BH*. An alternative method to evaluate *BH* is by employing the traditional Richardson or Arrhenius plot. To compute the activation energy, represented as $E_a = \Phi_{B0}$, we generated a $\ln(I_0/T^2)$ vs. q/kT plot, as illustrated in Fig. 3 [15, 16].

$$Ln\left(\frac{I_o}{T^2}\right) = \ln(AA^*) - \frac{q\Phi_{Bo}}{kT} \quad (4)$$

The values of E_a and A^* for Au/(PVC:Sm_2O_3)/n-Si structure were determined as 0.356 eV and 7.73×10^{-3} A/(cm·K)^2, respectively, extracted from the slope and intercept of the linear segment of the $\ln(I_0/T^2)$ versus q/kT curve. It is seen that this A^* value is approximately 1.45×10^4 times lower than its theoretical counterpart, which is 112.0 A/(cm·K)^2 for n-Si. Additionally, the value of E_a is lower than the mid-gap energy of Si. This discrepancy can be attributed to the reduced effective rectifier contact/diode area, a consequence of the presence of spatially distributed *BH* variations or potential fluctuations at the MS interface. In simpler terms, because of these potential *BH* fluctuations that encompass both lower and higher barrier regions, electron flow across the *BH* becomes preferentially biased toward these regions with lower *BH*, like patches. Recent literature has started to shed light on these disparities, including the differences between theoretical and practical A^* values, higher n values, and the non-linear trends in the conventional Richardson plot [17]. The lateral heterogeneity in the *BH* likely plays a role in influencing the determined A^* value from the *I–V–T* characteristics. As the temperature increases, the increased size of the homogeneous region compensates for the lower BH of the patches at the MS interface, thereby directing most of the current flow through it.

As shown in Fig. 4, the value of *n* was observed to be inversely proportional to the increasing temperature according to the equation: $n(T) = n_0 + T_0/T$. Here, n_0 and T_0 represent constants, with values of 3.0 and 1442 K, respectively. The variation of *n* with temperature, displaying an increase with decreasing temperature, is commonly referred to as the anomaly effect [2].

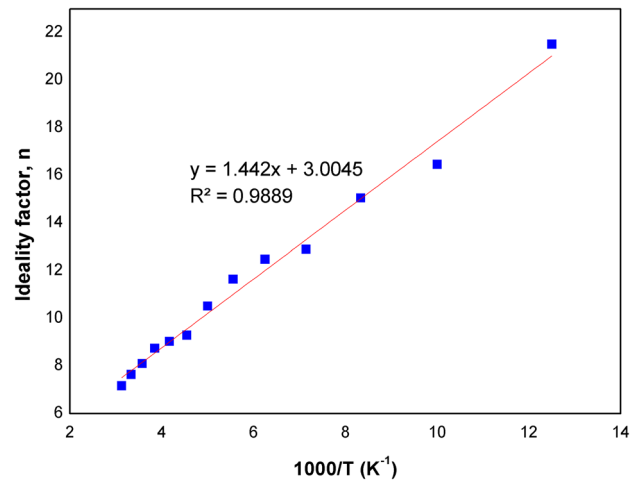

Fig. 4 The *n* vs 1000/*T* curve of the Au/(PVC:Sm_2O_3)/n-Si structure

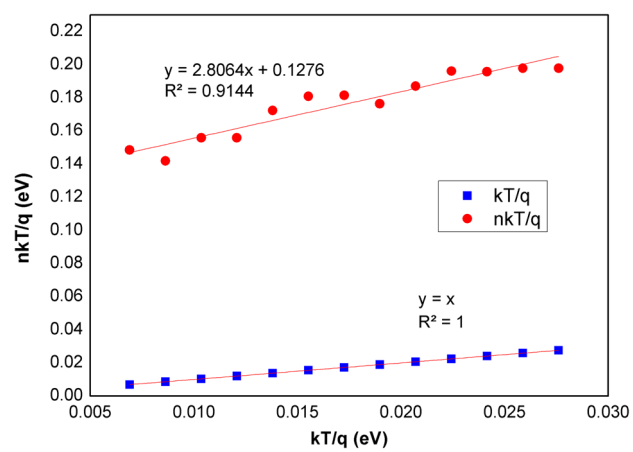

Fig. 5 The (kT/q) and $n.(kT/q)$ versus 1000/*T* curves of the Au/(PVC:Sm_2O_3)/n-Si structure

To assess the efficacy of the Thermionic Field Emission (TFE) and Fowler–Nordheim Field Emission (FE) mechanisms, a curve of $n.(kT/q)$ vs. kT/q was generated and is presented in Fig. 5. Both Table 1 and Fig. 5 reveal that neither FE nor TFE mechanisms serve as effective conduction mechanisms, as the values of $n.T$ or $n.(kT/q)$ are non-constant and demonstrate a linear increase with increasing temperature.

Conversely, E_{00} is the specified characteristic energy that measures the role of tunneling in conduction. E_{00} encompasses tunneling characteristics, including thermionic-field emission (TFE) and field emission (FE). It is linked to the transmission probability of charge

carriers through the barrier, as defined in relevant references [1, 2, 23]. The equation for E_{00} is:

$$E_{00} = (\hbar/4\pi)[N_D/(m_e^*\varepsilon_s\varepsilon_o)]^{0.5} \quad (5)$$

Equation 5 incorporates several parameters, where $\hbar$, N_D, m_e^*, ε_s, and ε_0 denote Planck's constant, the donor atom doping concentration, the effective mass of electrons, the dielectric constant of silicon ($\varepsilon_s = 11.8$), and the vacuum permittivity ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), respectively. By employing Eq. 5, the theoretical value of E_{00} was computed as 0.17 meV, a value significantly lower than the thermal energy at each measured temperature. However, upon experimental assessment of Fig. 5, the observed value was determined to be 127.6 meV, notably higher than the theoretical estimate. This discrepancy between the theoretical and experimental E_{00} values can be attributed to the lateral non-uniformity of the *BH* and localized enhancements in the electric field, resulting in a *BH* reduction within specific regions [24]. Additionally, the elevated n values recorded at each temperature cannot be solely accounted for by the TFE and FE mechanisms. Rather, factors such as the presence of an interlayer, surface states, and the donor atom concentration (8.62×10^{14} cm^{-3}) must also be taken into consideration.

To explain this conduct, we have examined the TE mechanism by integrating a Gaussian distribution (GD) of BHs, thereby accommodating the existence of localized regions or patches with lower BHs at the MS interface or BH non-uniformities. Tung [14] has illustrated that discrete regions or patches characterized by lower BHs within a higher, more uniform BH background result in an overall increase in BH with rising temperature. Expanding upon this concept, Mönch et al. [11] established a linear correlation between Φ_{B0} and n. It has been postulated that the Gaussian distribution of BHs across the Schottky contact area, encompassing parameters such as the mean BH and standard deviation (σ_0), provides an explanatory framework for the observed elevation in Φ_{B0} and the concurrent reduction in n with increasing temperature [25, 26].

In accordance with this theoretical framework, the *BH* derived from experiments signifies the apparent barrier height ($\Phi_{ap} = \Phi_{B0}$), and the ideality factor corresponds to the apparent value of n (n_{ap}), rather than the true value. To compute the standard deviation from the mean *BH*, the ensuing relationship can be employed [16, 17]:

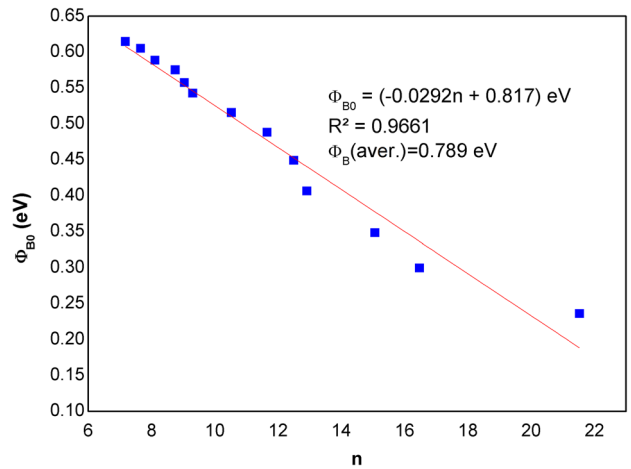

Fig. 6 The temperature-dependent experimental Φ_{B0} versus n curve was generated for the Au/(PVC: Sm_2O_3)/n-Si structure

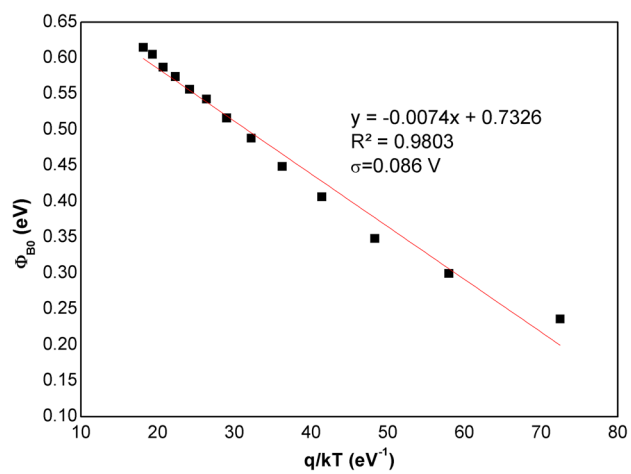

Fig. 7 The temperature-dependent experimental Φ_{B0} versus $q/2kT$ curve was generated for the Au/(PVC: Sm_2O_3)/n-Si structure

$$\Phi_{ap} = \Phi_{Bo} - \frac{q_{s0}^{\sigma 2}}{2kT} \quad (6)$$

Consequently, to ascertain the existence of a Gaussian distribution (GD) of BHs, we systematically generated and illustrated both the Φ_{B0} versus n and Φ_{B0} versus $q/(2kT)$ plots, as displayed in Figs. 6 and 7, respectively.

The figures presented clearly exhibit a robust linear relationship between both Φ_{B0} and n as well as Φ_{B0} and $q/2kT$. Consequently, by extrapolating the Φ_{B0} versus n curve to $n = 1$, we derived a mean value of 0.789 eV for the BH. Moreover, Fig. 7 demonstrates a consistent linear behavior within the temperature range of 80-320 K,

yielding $\overline{\Phi}_{B0}$ and σ_{s0} values of 0.732 eV and 0.086 V, respectively. The relatively non-negligible magnitude of σ_{s0} compared to $\overline{\Phi}_{B0}$provides further evidence of interface inhomogeneities.

The comprehensive findings collectively signify that the experimentally determined value of A^*, as derived from the conventional Richardson plot, deviates significantly from its theoretical counterpart. Moreover, the *BH* value extracted from the slope of this plot is notably lower than the mean *BH* value. These observations strongly imply that the effective active region of the diode is substantially smaller than its rectifier contact area, primarily due to the presence of spatial *BH* irregularities and potential fluctuations occurring at the MS interface. These irregularities encompass both lower and higher *BH* zones, or patches. Consequently, the transport of current across the diode is likely to exhibit a preferential flow through these lower barrier or patch regions, particularly at lower temperatures [27]. In consideration of these findings, we have constructed a modified Richardson curve (depicted in Fig. 8) by integrating the zero-standard deviation (σ_0) obtained from the slope of Φ_{B0} versus $q/2kT$ (Fig. 7), as follows:

$$Ln\left(\frac{I_0}{T^2}\right) - \frac{1}{2}\left(\frac{q\sigma_{so}}{kT}\right)^2 = Ln\left(AA^*\right) - \frac{q\overline{\Phi}_{Bo}}{kT} \quad (7)$$

The modified Richardson plot, depicted in Fig. 8, exhibits a consistent linear behavior across the entire measured temperature range. The values of $\overline{\Phi}_{B0}$and A^* for the Au/(PVC: Sm_2O_3)/n-Si structure were determined as 0.730 eV and 111.4 A/(cmK)^2, respectively, based on the slope and intercept of this plot. Remarkably, the experimental value of the effective Richardson constant closely matches its theoretical value of 112.0 A/(cmK)^2 for n-type Si. Additionally, the obtained $\overline{\Phi}_{B0}$values from the Φ_{B0}-n (Fig. 6), Φ_{B0}-$q/2kT$ (Fig. 7), and $Ln\left(\frac{I_0}{T^2}\right) - 0.5\left(\frac{q\sigma_{so}}{kT}\right)^2$vsq/kT (Fig. 8) curves are in agreement with each other. We can assert with confidence that the temperature dependence of the forward bias *I-V* characteristics of the Au/(PVC:Sm_2O_3)/n-Si structure, can be effectively explained using the Thermionic Emission (TE) theory with a single Gaussian distribution of BHs across the entire temperature range of measurement.

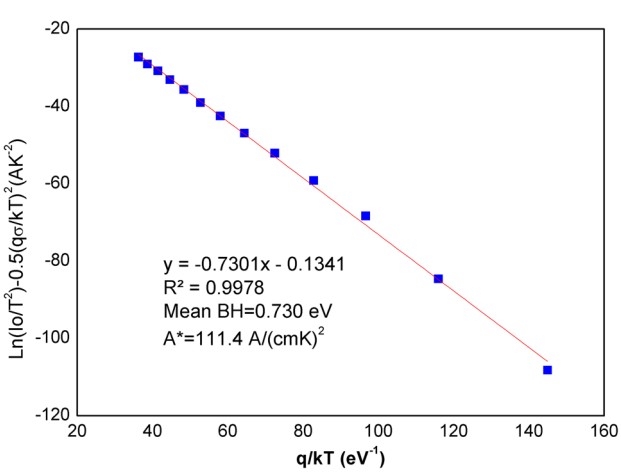

Fig. 8 The modified Richardson curve for the Au/(PVC: Sm_2O_3)/n-Si structure

The observed increase in BH with increasing temperature contradicts the typical behavior of a material's forbidden energy gap, characterized by a negative temperature coefficient of bandgap (α(Si) = dEg/dT = -4.73 × 10^{-4} eV/K). This unexpected trend can be attributed to the presence of surface states (N_{ss}), certain dislocations, cleaning, or surface preparation processes, as well as the Gaussian distribution of BHs. These surface states or traps act as recombination centers, capturing or emitting electrons and exerting a significant influence on the *I-V* characteristics. Understanding the energy-dependent profile of N_{ss} over a wide temperature range is of great importance. The existence of N_{ss} is commonly attributed to defects in the semiconductor surface and bulk, such as oxygen vacancies, shallow states related to the acceptor or donor atom concentration (doping level), and unsaturated dangling bonds [1, 2]. As a result, these surface states are more pronounced in their effects on the diode's behavior. According to Card and Rhoderick, a distinct energy-dependent profile for the density of N_{ss} can be described by incorporating the voltage-dependent ideality factor n(V) and the effective barrier height (Φ_e). This can be achieved through the utilization of the subsequent relationships. [28].

$$n(V) = \frac{q}{kT}(V/Ln\left(\frac{I_i}{I_0}\right) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (8a)$$

$$\Phi_e(V) = \Phi_{Bo} + \left[\left(1 - \frac{1}{n(V)}\right)V\right] \quad (8b)$$

Within Eq. 8 (a,b), the variables δ, ε_i, ε_s, and W_D denote the interlayer thickness, dielectric constant of

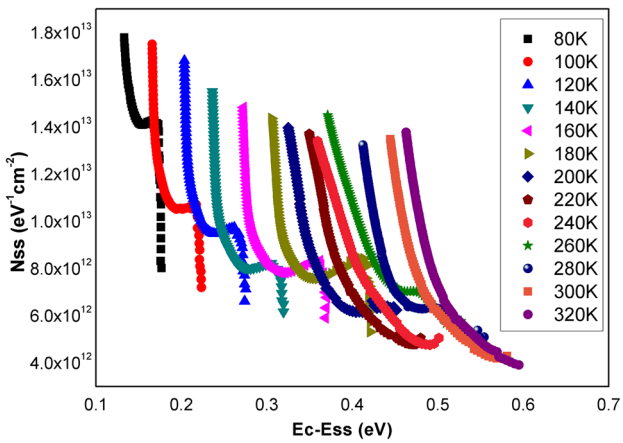

Fig. 9 The relationship between N_{ss} and E_c-E_{ss} for the Au/(PVC: Sm_2O_3)/n-Si structure

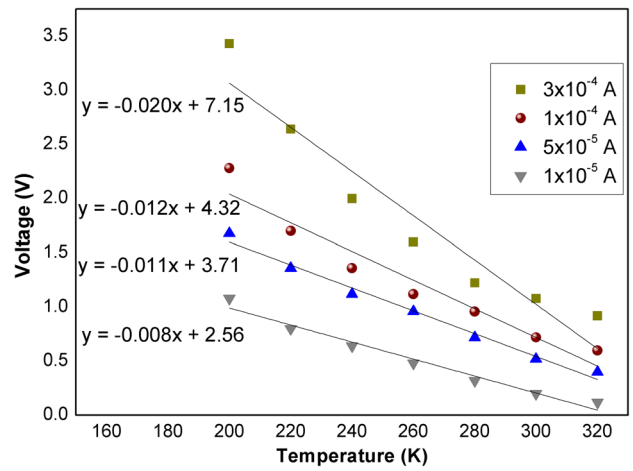

Fig. 10 The variations of V with temperature (T) for the Au/(PVC:Sm_2O_3)/n-Si structure under different electrical current conditions

the interlayer, dielectric constant of the semiconductor (where $\varepsilon_s = 11.8\ \varepsilon_0$ and $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm), and the thickness of the depletion layer, which is ascertained from the linear segment of the reverse bias C^{-2} versus V curve at sufficiently high frequencies [1, 2]. The relationship governing the conduction band (E_c) and E_{ss} for n-type semiconductors is articulated as [28]:

$$(E_c - E_{ss}) = q(\Phi_e - V) \tag{9}$$

Consequently, utilizing Eqs. 8 and 9, the energy-dependent profiles of N_{ss} are derived for each temperature and are visually represented in Fig. 9.

As shown in Fig. 9, both the magnitude and energy positions of N_{ss} undergo significant variations with temperature, as they undergo restructuring and reordering under the combined influence of temperature and electric field [27, 28]. As the temperature increases, the values of N_{ss} decrease, displaying an almost exponential rise from the midgap energy band towards the bottom of the E_C (Conduction Band Edge). These values fall within the range of 4.0×10^{12} eV^{-1}/cm^2 to 18×10^{12} eV^{-1}/cm^2, making them highly suitable for Schottky structures.

The sensitivity (S) is determined by analyzing the slope of the voltage-temperature (V-T) plots, and it is precisely defined as the temperature derivative of Eq. (10). Nevertheless, attaining both high sensitivity and maintaining a linear output over a wide temperature range can pose challenges when employing the Schottky structure of the metal–semiconductor (MS) and metal–insulator-semiconductor (MIS) varieties.

$$V = R_s I + n\Phi_n + (nkT/q).\ln\left(I/\left(AA^*T^2\right)\right) \tag{10}$$

Experimentally, the sensitivity value (S) for a temperature sensor based on the Au/(PVC: Sm_2O_3)/n-Si was assessed under the structure drive mode, maintained constant throughout the evaluation. To determine the temperature sensitivity of the fabricated Au/(PVC: Sm_2O_3)/n-Si, V versus T curves were plotted for four different forward currents, as illustrated in Fig. 10. It is evident from Fig. 10 that the temperature coefficient of voltage ranged from 7.86 mV/K to 20.4 mV/K, indicating that the fabricated Au/(PVC:Sm_2O_3)/n-Si exhibits high sensitivity to temperature, making it suitable for thermal sensor applications.

4 Conclusions

The I-V characteristics of the manufactured Au/(PVC: Sm_2O_3)/n-Si structure were examined in this work throughout a broad temperature range from 80 to 320 K. The conventional Richardson plot ($\ln(I_0/T^2)$-q/kT) displayed significant deviations from linearity at low temperatures, and the obtained value of A^* (7.73×10^{-3} A.cm^{-2} K^{-2}) was remarkably lower than its theoretical counterpart. The reduction in the value of R_s with increasing temperature can be attributed to the decrease in the forbidden bandgap (E_g) and the subsequent increase in conductivity. As a result, we constructed a modified Richardson plot,

employing the obtained zero standard deviation (σ_0) from the slope of Φ_{B0} versus $q/2kT$. Remarkably, both the magnitude and energy positions of N_{ss} exhibited significant variations with temperature due to structural reorganization and reordering induced by temperature and electric field effects. This observation further emphasized the intricate interplay between temperature and the characteristics of the fabricated structure. Furthermore, the temperature sensitivity of this structure was evaluated using V versus T curves under four different forward current conditions, yielding values ranging from 7.86 to 20.4 mV/K. This remarkable sensitivity to temperature suggests that the Au/(PVC:Sm_2O_3)/n-Si structure can serve as an excellent candidate for thermal sensor applications. These findings provide valuable insights for designing temperature-sensitive devices using this novel Schottky structure.

Author contributions

YB: Conceptualization, Methodology, Investigation, Data curation, Software, Visualization, Validation, Writing—Original Draft, Writing- Reviewing and Editing. HA: Conceptualization, Methodology, Investigation, Data curation, Software, Visualization, Validation, Writing—Original Draft ŞA: Conceptualization, Methodology, Investigation, Data curation, Validation, Writing—Original Draft, Writing- Reviewing and Editing.

Funding

Open access funding provided by the Scientific and Technological Research Council of Türkiye (TÜBİTAK).

Data availability

The data that support the findings of this study are available from the corresponding author, upon reasonable request.

Declarations

Competing interests The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethical approval All procedures performed in studies were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards.

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References

1. S.M. Sze, *Physics of semiconductor devices*, 2nd edn. (Wiley, New York, 1981)
2. B.L. Sharma, *Metal-semiconductor Schottky barrier junctions and their applications* (Plenum Press, New York, 1984)
3. F.A. Padovani, R. Stratton, Field and thermionic-field emission in Schottky barriers. Solid-State Electron. **9**, 695–707 (1966)
4. K. Sreenu, C. Venkata Prasad, V. Rajagopal Reddy, Barrier parameters and current transport characteristics of Ti/p-InP Schottky junction modified using orange G (OG) organic interlayer. J. Electron. Mater. **46**, 5746–5754 (2017)
5. V. Rajagopal Reddy, V. Manjunath, V. Janardhanam, Y.-H. Kil, C.-J. Choi, Electrical properties and current transport mecahnism of the Au/n-GaN Schottky structure with

solution-processed high-k $BaTiO_3$ interlayer. J. Electron. Mater. **43**, 3499–3507 (2014)
6. H. Ertap, H. Kacus, S. Aydogan, M. Karabulutd, Analysis of temperature dependent electrical characteristics of Au/GaSe Schottky barrier diode improved by Ce-doping. Sens. Actuators, A **315**, 112264 (2020)
7. J. Werner, H. Guttler, Barrier inhomogeneities at Schottky contacts. J. Appl. Phys. **69**, 1522 (1991)
8. B. Prasanna Lakshmi, M.S.P. Reddy, A. Ashok Kumar, V. Rajagopal Reddy, Electrical transport properties of Au/SiO_2/n-GaN MIS structure in a wide temperature range. Curr. Appl. Phys. **12**, 765–772 (2012)
9. J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, Electron transport of inhomogeneous Schottky barriers: a numerical study. J. Appl. Phys. **70**, 7403 (1991)
10. Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, On the difference in apparent barrier height as obtained from capacitance-voltage and current-voltage-temperature measurements on Al/p-InP Schottky barriers. Solid-States Electron. **29**, 633–638 (1986)
11. W. Mönch, J. Vac, Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities. Sci. Technol. B **17**, 1867 (1999)
12. R.F. Schmitsdorf, T.U. Kampen, W. Mönch, Correlation between barrier height and interface structure of Ag/Si (111) Schottky diodes. Surf. Sci. **324**, 249 (1995)
13. M.S.P. Reddy, Hee-Sung. Kang, V. Jung-Hee Lee, Rajagopal Reddy, Ja-Soon. Jang, Electrical Properties and the Role of Inhomogeneities at the PolyvinylAlcohol/n-InP Schottky barrier interface. J. Appl. Polym. Sci. **131**, 39773 (2014)
14. R.T. Tung, Recent advances in Schottky barrier concepts. Mater. Sci. Eng. R **35**, 1 (2001)
15. H. Durmuş, A. Tataroğlu, Ş Altındal, M. Yıldırım, The effect of temperature on the electrical characteristics of Ti/n-GaAs Schottky diodes. Curr. Appl. Phys. **44**, 85–89 (2022)
16. S. Demirezen, S. Altındal Yerişkin, A detailed comparative study on electrical and photovoltaic characteristics of Al/p-Si photodiodes with coumarin-doped PVA interfacial layer: the effect of doping concentration. Polym. Bull. **77**, 49–71 (2020)
17. Ş Karataş, Ş Altındal, M. Ulusoy, Y. Azizian-Kalandaragh, S. Özçelik, Temperature dependence of electrical characteristics and interface state densities of Au/n-type Si structures with SnS doped PVC interface. Phys. Scr. **97**, 095816 (2022)
18. H.G. Çetinkaya, O. Çiçek, Ş Altındal, Y. Badali, S. Demirezen, Vertical CdTe:PVP/p-Si—based temperature sensor by using aluminum anode Schottky contact. IEEE Sens. J. **22**, 22391–22397 (2022)
19. A.A. Alsaç, T. Serin, S.O. Tan, Ş Altındal, Identification of current transport mechanisms and temperature sensing qualifications for Al/(ZnS-PVA)/p-Si structures at low and moderate temperatures. IEEE Sens. J. **22**, 99–106 (2021)
20. Ş Altındal, A. Barkhordari, S. Özçelik, G. Pirgholi-Givi, A comparison of electrical characteristics of Au/n-Si (MS) structures with PVC and (PVC:Sm_2O_3) polymer interlayer. Phys. Scr. **96**, 125838 (2021)
21. Ş Altındal, A. Barkhordari, Y. Azizian-Kalandaragh, B.S. Çevrimli, H.R. Mashayekhi, Dielectric properties and negative-capacitance/dielectric in Au/n-Si structures with PVC and (PVC:Sm_2O_3) interlayer. Mater. Sci. Semicon. Process. **147**, 106754 (2022)
22. E. Evcin Baydilli, Ş Altındal, H. Tecimer, A. Kaymaz, H. Uslu Tecimer, The determination of the temperature and voltage dependence of the main device parameters of Au/7% Gr-doped PVA/n-GaAs-type Schottky Diode (SD). J. Mater. Sci. Mater. Electron. **31**, 17147–17157 (2020)
23. G. Greco, P. Fiorenza, M. Spera, F. Giannazzo, F. Roccaforte, Forward and reverse current transport mechanisms in tungsten carbide Schottky contacts on AlGaN/GaN heterostructures. J. Appl. Phys. **129**, 234501 (2021)
24. Z.J. Horváth, Comment on analysis of IV measurements on $CrSi_2$-Si Schottky structures in a wide temperature range. Solid State Electron. **39**, 176 (1995)
25. S. Duman, A. Turut, S. Dogan, Thermal sensitivity and barrier height inhomogeneity in thermally annealed and un-annealed Ni/n-6H-SiC Schottky diodes. Sens. Actuators, A **338**, 113457 (2022)
26. H. Efeoğlu, A. Turut, Current-voltage-measurement temperature characteristics depending on the barrier-forming contact metal thickness in Au/Cu/n-Si/Au–Sb/Ni rectifying contacts. Mater. Sci. Semicon. Process. **143**, 106532 (2022)
27. Ş Altındal, H. Kanbur, A. Tataroğlu, M.M. Bülbül, The barrier height distribution in identically prepared Al/p-Si Schottky diodes with the native interfacial insulator layer (SiO_2). Phys. B Condens. Matter **399**, 146–154 (2007)
28. H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. J. Phys. D: Appl. Phys. **4**, 1589 (1971)

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