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DEVELOPMENT AND CONTROL OF GAN-BASED PHASE SHIFTED FULL BRIDGE CONVERTER FOR MILITARY APPLICATIONS

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(M. Sc. Thesis)

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ABSTRACT

Today, military systems have great importance to ensure national security. As technology develops day by day, the development of superior performance military systems will continue. Military standards are used to develop systems and ensure they work in harmony with each other. MIL-STD-1760 and MIL-STD-704 are standards for military aircraft. This thesis focuses on designing and controlling a GaN-based Phase-Shifted Full Bridge converter that complies with these standards. For the designed DC-DC converter, it is explained how the power interface and input voltage range are determined according to these standards. The converter operates with an input voltage range of 200-400V and provides 500W of output power at 28V. The Phase-Shifted Full Bridge topology was chosen after comparing it with other types of converters. A detailed analysis of this topology is provided. To achieve high power density, a high switching frequency was chosen. GaN switches were selected for their ability to operate at high frequencies. The components in the power stage were chosen based on calculations. Voltage Mode Control and Current Mode Control were developed, and the design process for the controller is explained. MATLAB was used for the controller design. The converter was verified through LTspice and PLECS simulations. The results show that the converter works stably across the specified input voltage range and varying load conditions.

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ASKERİ UYGULAMALAR İÇİN GAN TABANLI FAZ KAYDIRMALI TAM KÖPRÜ DÖNÜŞTÜRÜCÜ GELİŞTİRİLMESİ VE KONTROLÜ

(Yüksek Lisans Tezi)

Selim BAYRAM

GAZİ ÜNİVERSİTESİ

FEN BİLİMLERİ ENSTİTÜSÜ

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ÖZET

Günümüzde askeri sistemler, ulusal güvenliği sağlamak için büyük öneme sahiptir. Teknolojinin her geçen gün gelişmesiyle birlikte, üstün performanslı askeri sistemlerin geliştirilmesi devam edecektir. Askeri standartlar, sistemlerin geliştirilmesi ve birbirleriyle uyumlu çalışmasını sağlamak için kullanılmaktadır. MIL-STD-1760 ve MIL-STD-704, askeri uçaklar için belirlenmiş standartlardır. Bu tez, bu standartlara uygun bir GaN tabanlı Faz Kaydırmalı Tam Köprü dönüştürücünün tasarımı ve kontrolüne odaklanmaktadır. Tasarlanan DC-DC dönüştürücü için, güç arayüzü ve giriş gerilim aralığının bu standartlara göre nasıl belirlendiği açıklanmıştır. Dönüştürücü, 200-400V giriş gerilim aralığında çalışmakta ve 28V çıkış geriliminde 500W güç sağlamaktadır. PSFB topolojisi, diğer dönüştürücü tipleriyle karşılaştırıldıktan sonra seçilmiştir. Bu topolojiye ilişkin detaylı bir analiz sunulmuştur. Yüksek güç yoğunluğu elde etmek için yüksek anahtarlama frekansı seçilmiştir. GaN anahtarları, yüksek frekansta çalışma yetenekleri nedeniyle tercih edilmiştir. Güç aşamasındaki bileşenler, hesaplamalar temel alınarak seçilmiştir. Gerilim Modu Kontrolü ve Akım Modu Kontrolü geliştirilmiş ve kontrolcü tasarım süreci açıklanmıştır. Kontrolcü tasarımı için MATLAB kullanılmıştır. Dönüştürücü, LTspice ve PLECS simülasyonlarıyla doğrulanmıştır. Simülasyon sonuçları ile, dönüştürücünün belirtilen giriş gerilim aralığında ve değişen yük koşullarında kararlı bir şekilde çalıştığını gösterilmiştir.

Bilim Kodu	:	93419
Anahtar Kelimeler	:	Askeri uygulama, faz kaydırmalı tam köprü dönüştürücü, GaN MOSFET, sıfır gerilim anahtarlama, güç elektroniği, gerilim modu kontrolü, akım modu kontrolü, yüksek frekans uygulamaları, güç yoğunluğu
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SYMBOLS AND ABBREVIATIONS

The symbols and abbreviations used in this study are presented below, along with their explanations.

Symbols	Explanations
C	Capacitance
D	Diode
Hz	Hertz
f	Frequency
I	Current
kHz	Kilohertz
L	Inductance
lk	Leakage
N	Turns Number
P	Power
Ph	Phase Shift
Ph_{eff}	Effective Phase Shift
R	Resistance
t	Time
V	Voltage

Abbreviations	Explanations
AC	Alternating Current
ACMC	Average Currnet Mode Control
BJT	Bipolar Junction Transistors
CMC	Current Mode Control
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
GaN	Gallium Nitride

Abbreviations	Explanations
FET	Field-Effect Transistor
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PWM	Pulse-Width Modulation
RDSon	On State Resistance
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SMPS	Switch Mode Power Supplies
VDS	Drain-Source Voltage
VGS	Gate-Source Voltage
VMC	Voltage Mode Control
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1. INTRODUCTION

MIL-STD-1760 is a standard that defines electrical interfaces used with military aircraft. Compliance with this standard ensures that the developed system operates reliably with military air platforms and ensures compatibility in power and communications connections. The connector pin assignments shown in Figure 1.1 represent the electrical interfaces specified by this standard.

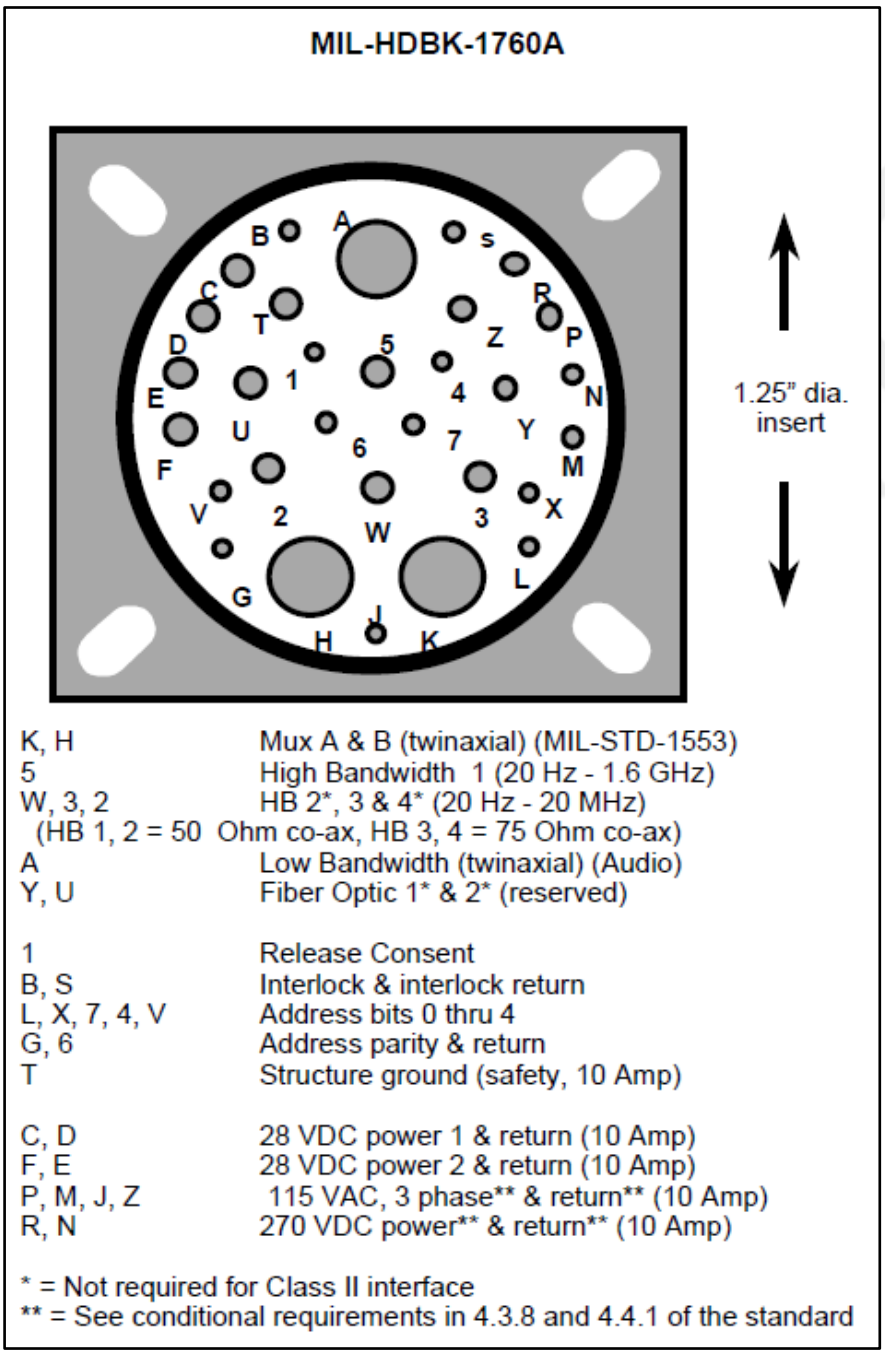

Figure 1.1. Electrical interface defined in MIL-STD-1760

As seen in Figure 1.1, MIL-STD-1760 represent several power interfaces to support various operational needs of systems connected to military aircraft. These include 28V DC, 270V DC, and 115V AC power interfaces. Each of these interfaces serves different power requirements and system designs. The 28V DC interface is used for lower power systems and auxiliary equipment until 280W according to standart. 270V DC and 115V AC power interfaces should be used for applications requiring higher power. In this study, it is aimed to develop a DC-DC converter for a system to be integrated into a military aircraft. Since the system requires 500W power, 270V DC or 115V AC power interface can be used. Within the scope of this study, 270V DC interface was preferred to supply the system.

On the other hand, MIL-STD-704 standard defines power quality and power distribution requirements for military aircraft. This standard specifies electrical requirements such as input voltage, frequency deviations and voltage regulation to ensure reliable and stable operation of the power system. Figure 1.2 shows the envelope of voltage transient for 270V DC power interface. This envelope was taken from MIL-STD-704.

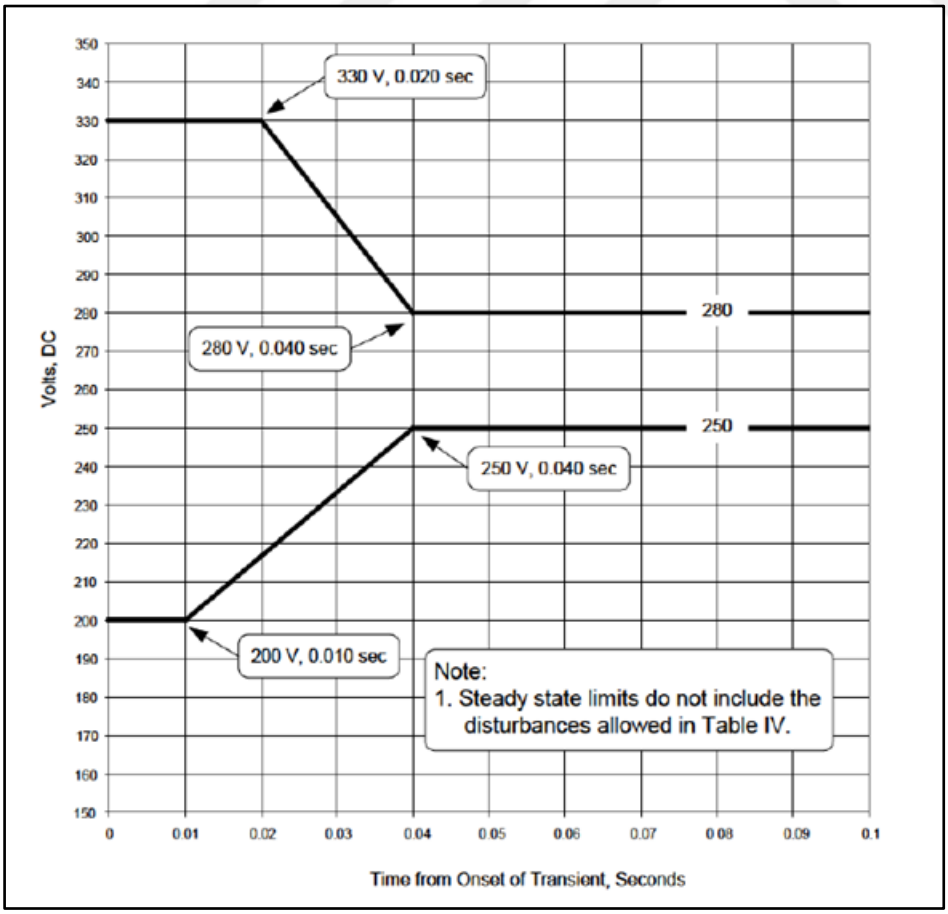

Figure 1.2. Envelope of voltage transient for 270V DC power interface.

The steady state voltage range for the 270V DC power interface is given as 250V to 280V. However, some transients may occur at the power interface under normal operating conditions. The standard limits these transient states as seen in Figure 1.2. The voltage envelope ranges from 200V to 330V. Within the scope of this study, it is aimed to develop a DC-DC converter that can operate without being affected by these transient conditions. Additionally, to address potential voltage overshoots, the input voltage range of the converter has been extended to from 200 to 400V.

DC-DC converters are power electronic circuits that convert a DC voltage to a different DC voltage level, often providing a regulated output. There are two methods for DC-DC conversion. First method is linear voltage regulation. Linear voltage regulators are inherently inefficient, especially when a significant difference exists between input and output voltages. For instance, if the output voltage is one-quarter of the input voltage, only 25 percent of the input power is delivered to the load, while the remaining 75 percent is dissipated as heat [1]. This inefficiency restricts their use to low-power applications. The other method of DC-DC conversion is switching mode regulation. They are efficient alternative of linear voltage regulators. These types of regulators are called switch mode power supplies (SMPS). SMPS are widely used in many applications such as automotive, military and so on. General structure of DC-DC converters that most used in literature is shown in Figure 1.3.

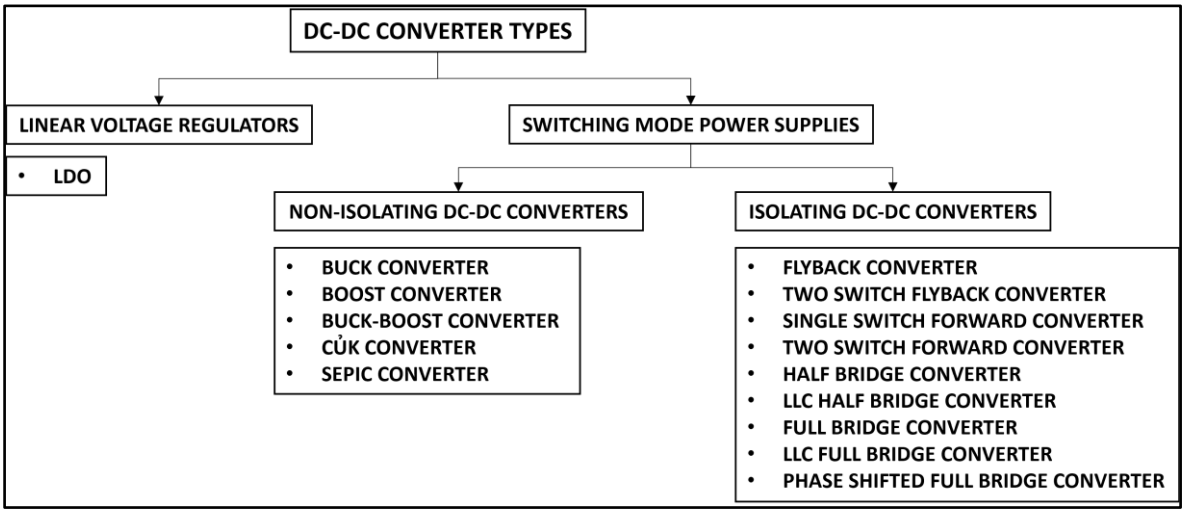

Figure 1.3. General structure of DC-DC converters

As the name suggests, SMPS rely heavily on the switching action of their main switching elements to regulate and convert voltage efficiently. The efficiency of an SMPS is

significantly influenced by the performance of the switching component. Several types of switching elements can be used in SMPS, such as Bipolar Junction Transistors (BJTs), Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). BJTs were once common in power conversion but have been largely replaced due to their slower switching speeds and higher losses. IGBTs are suitable for high-power and high-voltage applications with moderate switching frequencies but suffer from higher switching losses at higher frequencies. The most prevalent switches for medium to high-frequency applications are MOSFETs. They provide fast switching, low conduction losses, and efficient voltage control. Silicon-based (Si) MOSFETs work well for operating voltages typically below 600V.

However, traditional Si MOSFETs face limitations at higher voltages and higher frequencies. To overcome these challenges, Gallium Nitride (GaN) MOSFETs and Silicon Carbide (SiC) MOSFETs have emerged as an advanced alternative. Applications fields of Si, SiC, and GaN switching devices are shown in Figure 1.4. It is appropriate to use GaN MOSFET for this study.

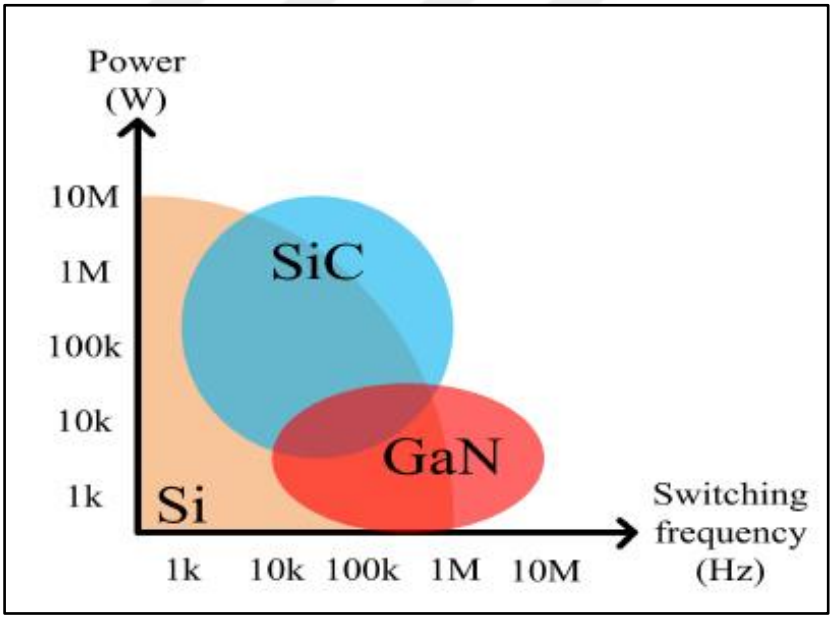

Figure 1.4. Applications fields of Si, SiC, and GaN switching devices

GaN is a wide bandgap semiconductor and offers advantages such as switching ability at high frequencies thanks to its lower parasitic capacitance compared to silicon-based MOSFETs. GaN devices also feature lower on-resistance, contributing to less power loss

during conduction. These attributes make GaN devices particularly suitable for high-frequency applications, where efficiency and thermal management are critical [2-5]. By enabling higher switching frequencies, GaN technology allows for smaller passive components and more compact power supply designs.

There are many topologies of SMPS in literature. One of them is the Phase Shifted Full Bridge Converter (PSFB). The PSFB converter is a well-established topology in medium to high-power applications, particularly valued for its ability to achieve zero-voltage switching (ZVS) [6,7]. ZVS significantly reduces switching losses by allowing the MOSFETs to turn on when the voltage across them is nearly zero, thereby minimizing the stress on the components and improving overall efficiency [6]. The integration of GaN MOSFETs into the PSFB topology further enhances the converter's performance, allowing operation at higher switching frequencies, which reduces the size of passive components and improves power density [8].

The purpose of this thesis is to develop and control a PSFB converter utilizing GaN MOSFETs. This design specifically to meet the demands of military applications. The converter operates at a high switching frequency of 500kHz and deliver an output power of 500W at 28V. To address the transient conditions defined in MIL-STD-704, the input voltage range is extended to 200–400V, ensuring the system operates reliably even during voltage overshoots. The focus of the control strategy is to keep the converter stable under varying input voltages and load conditions. In this study, while designing the controller, MATLAB was used to create the frequency responses. In this way, the controller was designed by evaluating system stability and dynamic response. LTspice and PLECS were utilized for the power stage design and its verification. LTspice was used for theoretical validation of component selection. PLECS enabled detailed simulation of the entire power stage and controller under various operating conditions.

2. TOPOLOGY SELECTION

The selection of an appropriate converter topology is crucial for the development of high-performance DC-DC converters but there is no simple procedure exists to select the right topology [9]. Topologies can be categorized in various ways, one of which is based on their switching technique: hard switching and soft switching. Each type comes with its distinct advantages and trade-offs.

2.1. Hard Swithcing Topologies

Hard switching refers to traditional switching methods. When semiconductor devices switch between on and off states, the voltage and current of the switch overlap. This overlap leads to switching losses and increased electromagnetic interference (EMI). The effect of this overlap is visualized in the current-voltage diagram given in Figure 2.1.

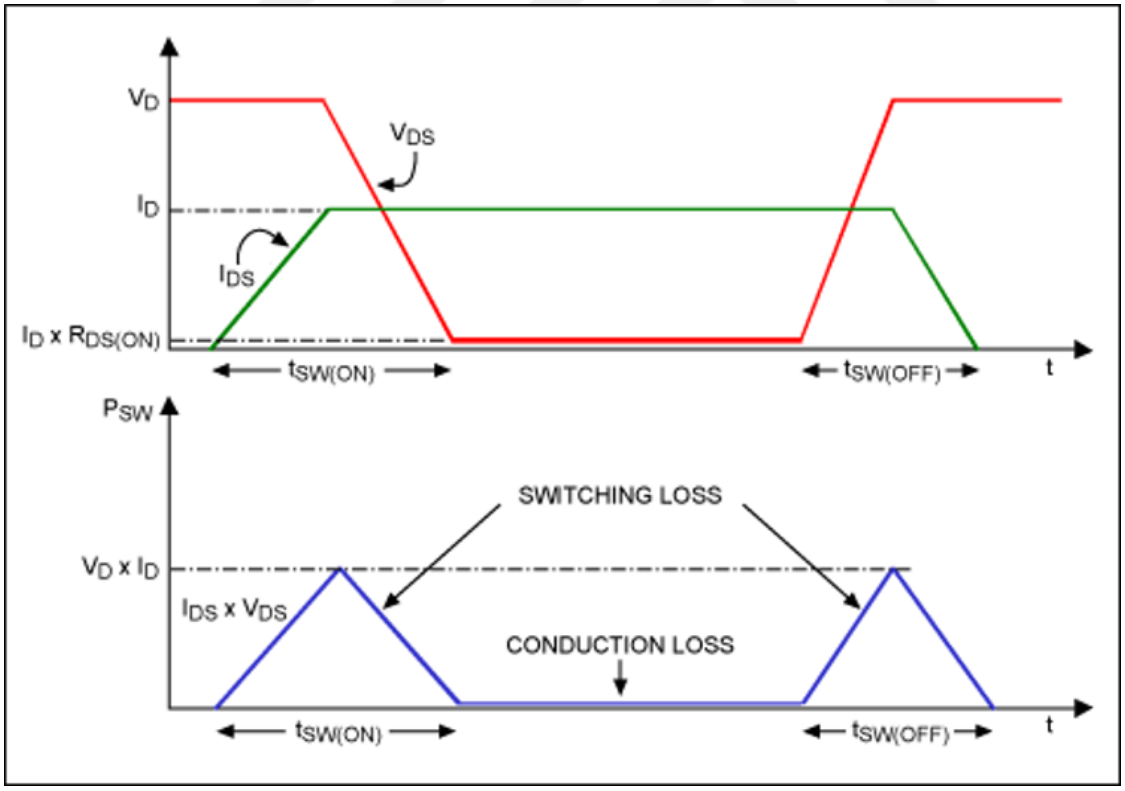

Figure 2.1. Switching loss visualization

Common hard-switching topologies is given in following subsections.

2.1.1. Flyback and forward converters

These simple topologies are suitable for low-power applications due to their straightforward design and low component count. However, when power levels exceed a few hundred watts, switching losses and magnetic losses become very high. They are impractical due to thermal management difficulties, especially in small areas. Flyback and Single Switch Forward converter circuit schema is given in Figure 2.2.

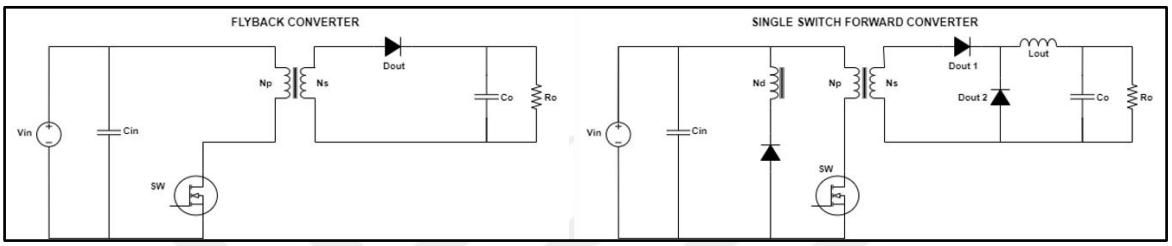

Figure 2.2. Flyback and single switch forward converter circuit schema

2.1.2. Half-bridge and full-bridge converters

These configurations offer better voltage distribution across switches. They are suitable for medium to high power levels but they need to more component count than Flyback and Forward converters. The Full-Bridge converter can manage higher power by utilizing all four switches for power transfer, but at higher switching frequencies, the hard-switching nature results in significant energy loss and heat generation. Figure 2.3 shows the conventional Full Bridge converter schema.

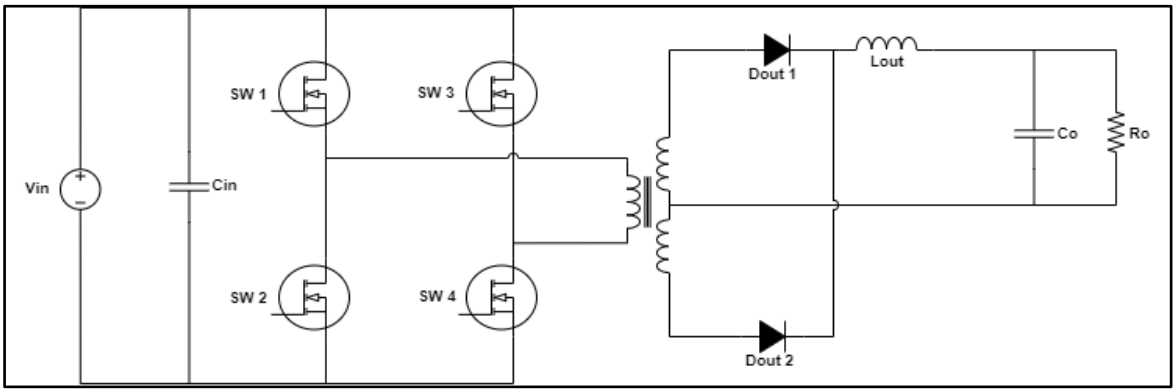

Figure 2.3. Conventional full bridge converter schema

2.2. Soft Switching Topologies

To mitigate the drawbacks of hard-switching, soft-switching techniques, Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) have been developed. These methods aim to minimize or eliminate voltage and current overlap during switching transitions. In this way, power losses and EMI are significantly reduced.

ZVS occurs when the switch transitions from the off state to the on state, ensuring that the voltage across the switch is zero at the moment of turn-on. Conversely, ZCS takes place when the switch transitions from the on state to the off state, ensuring that the current through the switch is zero at the moment of turn-off. Both techniques offer significant efficiency improvements and reduced thermal stress on switching devices. For better understanding, a visual representation of the ZVS and ZCS waveforms is given in Figure 2.4 and shows how these techniques enable lossless switching.

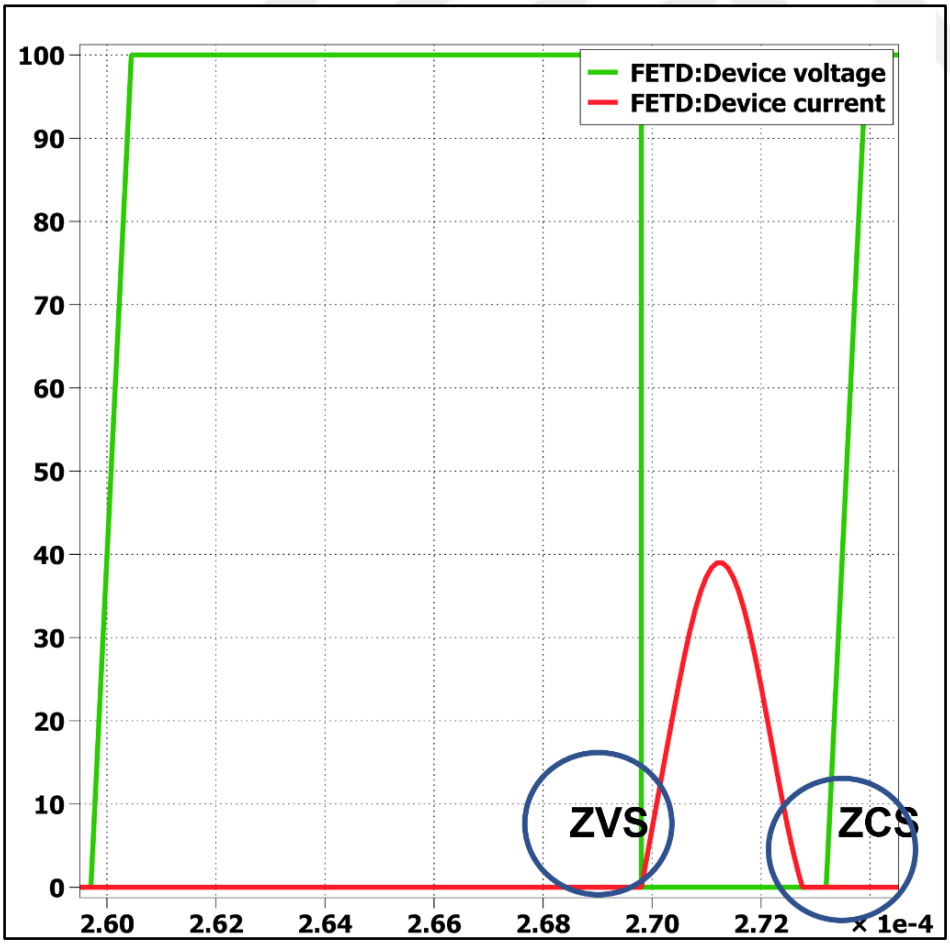

Figure 2.4. ZVS and ZCS waveforms

Examples of widely used soft-switching topologies is given in following subsections.

2.2.1. LLC resonant converter

The LLC Resonant converter is a popular soft-switching topology that leverages resonant tank circuits to achieve ZVS or ZCS operation. It is characterized by a series inductor and capacitor network, which allows controlled resonance during switching transitions. The resonant operation ensures minimal overlap between voltage and current, significantly improving efficiency. LLC Resonant converter can be non-isolate or isolate. All type of resonant converter has inverter section (half bridge or full bridge) and LLC tank section. The output voltage is controlled by the change of frequency. Figure 2.5 shows a full bridge LLC Resonant Converters with center-tapped rectifier circuit scheme.

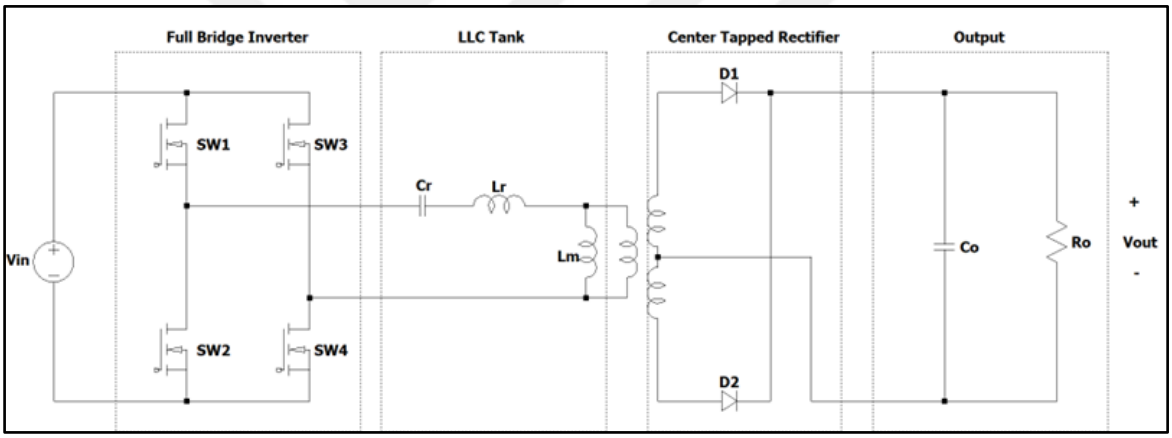

Figure 2.5. The circuit scheme of full bridge LLC resonant converter with center-tapped rectifier

LLC converters are commonly employed in applications requiring high efficiency, compact design, and low EMI. Due to their ability to operate over a wide load range, they are widely used in data centers, telecommunications, and industrial power supplies.

2.2.2. PSFB converter

The PSFB converter is another soft-switching topology that utilizes ZVS to minimize switching losses. It uses conventional Full-Bridge configuration with the added advantage of ZVS. In this topology, the primary-side switches of the full-bridge configuration are

controlled with phase shifts. This phase shift determines the timing of transitions between different states of the converter, which allows the output voltage to be controlled. The key advantage of the PSFB topology lies in its ability to achieve ZVS, thereby reducing switching losses and improving efficiency [6,10]. During each switching cycle, the energy stored in the leakage inductance of the transformer and the parasitic capacitance of the switches are utilized to create a resonant transition. This transition allows the voltage across the switches to reach zero before they are turned on, minimizing the energy dissipated during switching [6]. PSFB converters are effective in medium-to-high power applications. Figure 2.6 below illustrates the basic schematic of a PSFB converter with current doubler rectifier, highlighting the primary and secondary side components, including the transformer, rectifier diodes, and filter components.

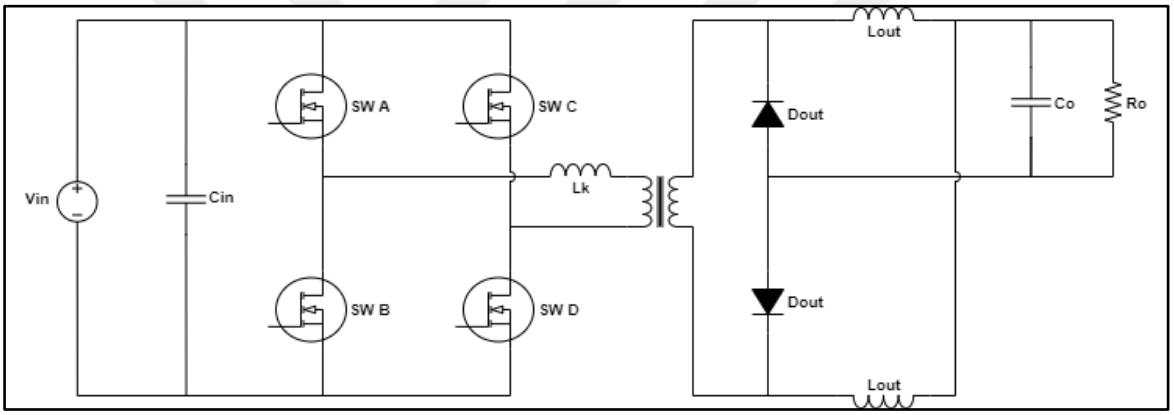

Figure 2.6. The circuit scheme of PSFB converter with current doubler rectifier

To achieve high power density, the switching frequency must be high. As the switching frequency increases, switching losses will naturally increase. In order to reduce these losses, it was decided to use a converter topology with soft switching method in this study. After examining the 2 most popular topologies, the PSFB topology was chosen because it operates at a fixed frequency. The following sections will detail the analysis and design of the PSFB converter, highlighting the component selection and control strategy.

3. DETAILED ANALYSIS OF PSFB

In this chapter, the operation of the PSFB converter is analyzed in detail, focusing on the 10 distinct modes that occur during one switching period [11]. The PSFB topology uses phase-shift modulation to regulate output voltage. It comprises four primary switches arranged in an H-bridge configuration, with complementary pairs (A-B and C-D) operating with a 50% duty cycle and a small dead time to facilitate ZVS. The phase shift between these pairs controls the energy transferred to the load. The gate signals of swithces and modes of operation in one switching cycle are shown in Figure 3.1. It also shows primary and secondary voltage of transformer.

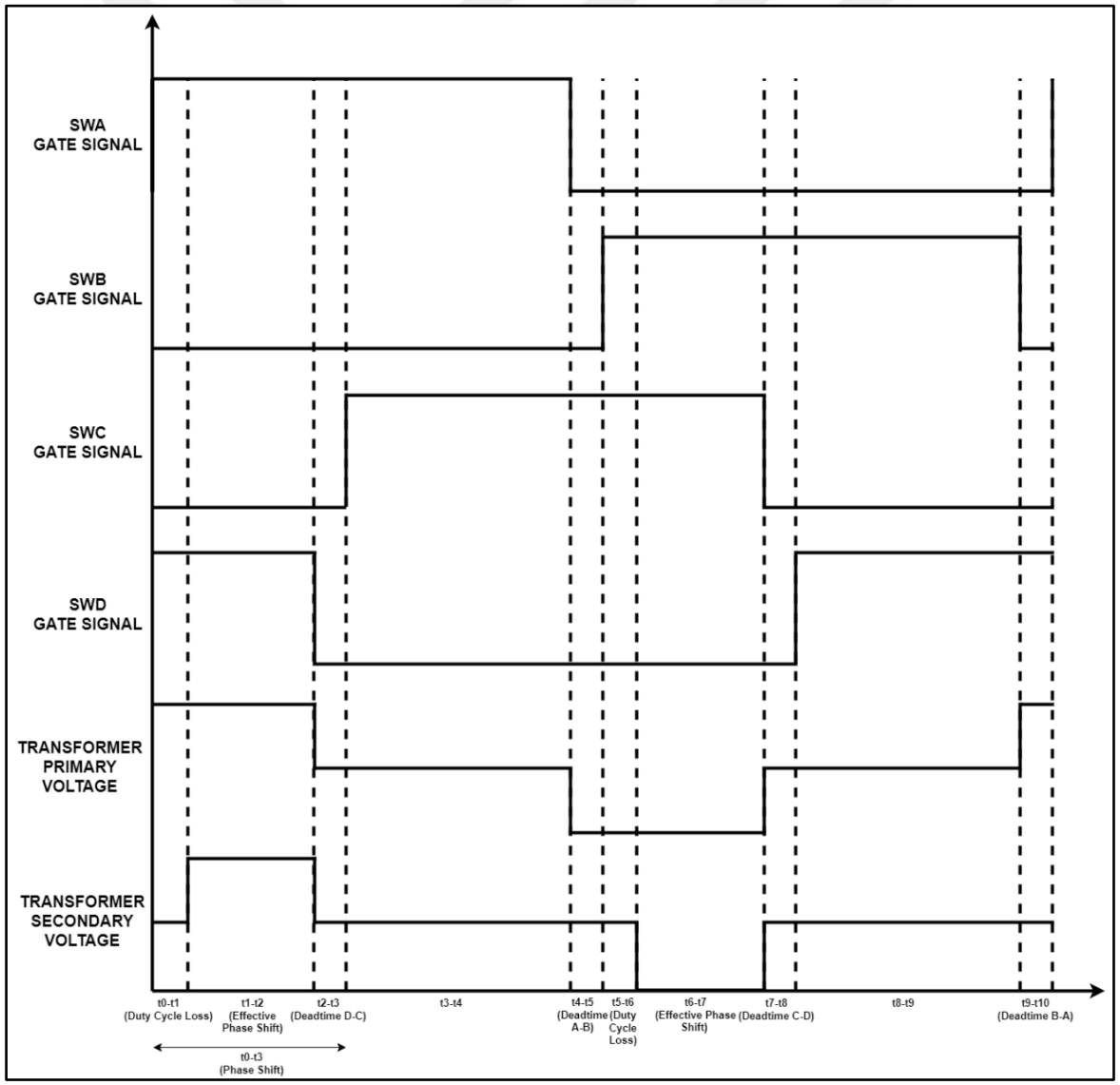

Figure 3.1. Modes of operation of PSFB

3.1. Mode 1 (t0 – t1)

At t0, switch A turns on with ZVS. During this mode, the transformer secondary voltage remains zero, and both secondary diodes conduct, allowing the output inductors to discharge. The primary current begins reversing direction, charging the leakage inductance. No energy is transferred from the primary to the secondary side until the leakage inductance current, multiplied by the transformer turns ratio, equals the output inductor current. Consequently, the transformer secondary voltage remains zero. This period is referred to as the "Duty Cycle Loss Mode", with the effective phase shift calculated by subtracting this time and the dead time from the overall phase shift. Mode 1 is illustrated in Figure 3.2.

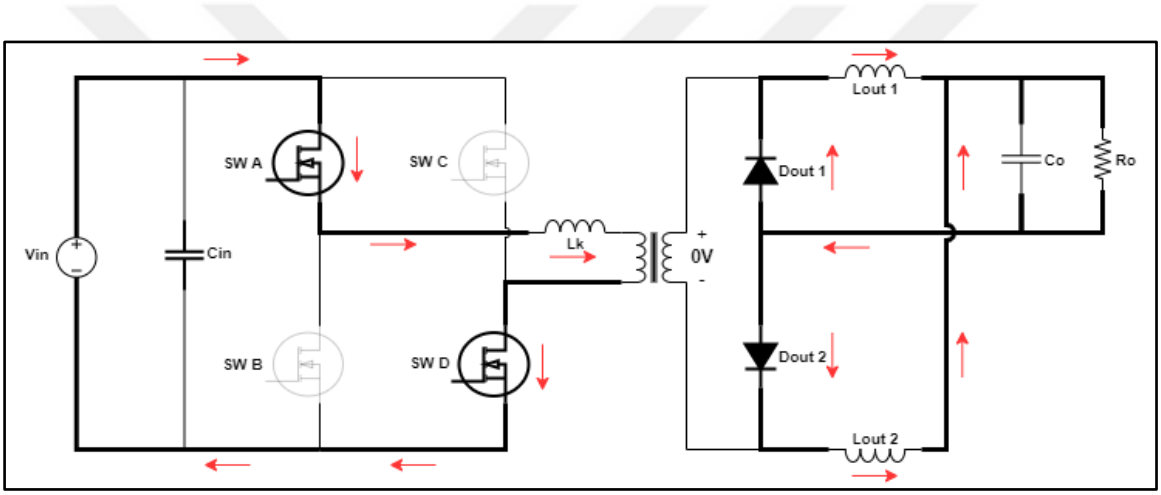

Figure 3.2. PSFB mode 1 (t0 – t1)

3.2. Mode 2 (t1 – t2)

At t1, the transformer secondary voltage rises to the input voltage multiplied by the transformer turns ratio, initiating power delivery to the load. Inductor Lout 1 begins charging, while Lout 2 discharges. Current flows through Dout 2, transferring energy to the output. In this mode, the effective phase shift starts. The current waveform for Mode 2 is shown in Figure 3.3.

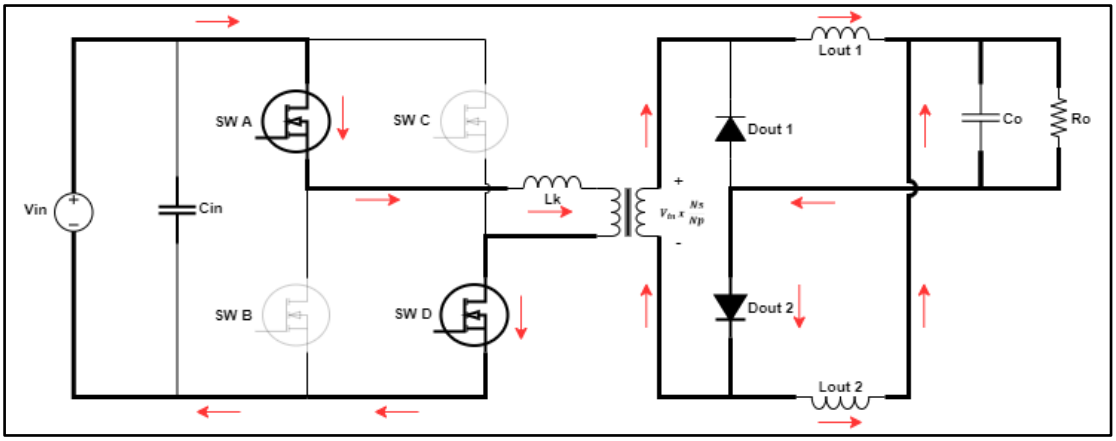

Figure 3.3. PSFB mode 2 (t1 – t2)

3.3. Mode 3 (t2 – t3)

At t2, switch D turns off, and the primary current charges the parasitic capacitance of switch D while discharging that of switch C. This period, known as the dead time between switches D and C, is required for switch C to achieve ZVS by fully discharging its parasitic capacitance. During this mode, both output diodes continue to conduct, the transformer secondary voltage remains zero, and no energy is transferred to the secondary side. The output inductors discharge throughout this period. Mode 3 is illustrated in Figure 3.4.

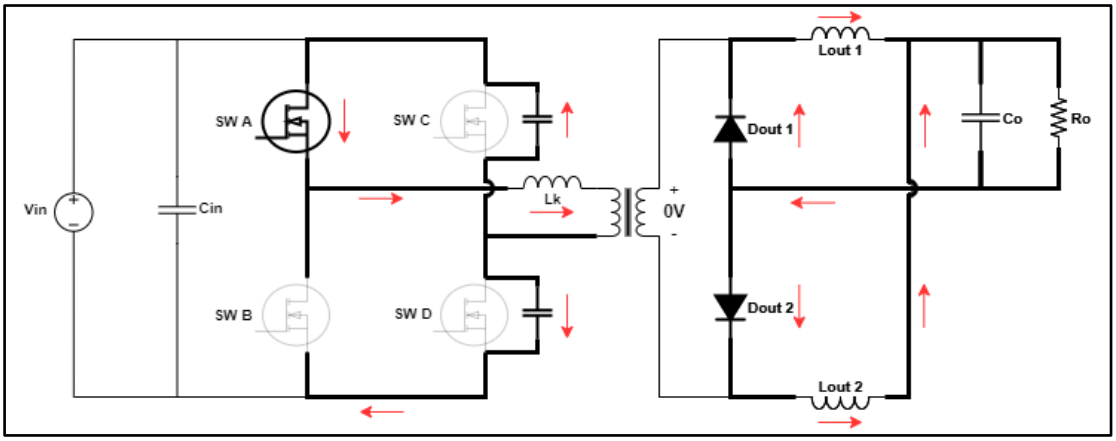

Figure 3.4. PSFB mode 3 (t2 – t3)

3.4. Mode 4 (t3 – t4)

At t3, switch C turns on with ZVS. The primary current freewheels through switches A and C, while the transformer secondary voltage remains zero. During this time, inductors Lout

1 and Lout 2 continue to discharge through the output diodes. Mode 4 is shown in Figure 3.5.

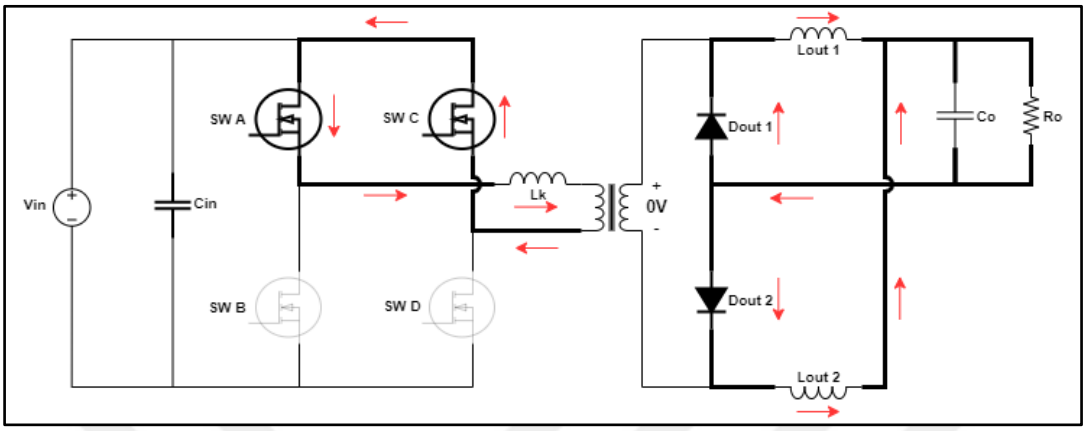

Figure 3.5. PSFB mode 4 (t3 – t4)

3.5. Mode 5 (t4 – t5)

At t4, switch A turns off, and the primary current charges the capacitance of switch A while discharging that of switch B. This period, known as the dead time between switches A and B, allows switch B to achieve ZVS by fully discharging its parasitic capacitance. During this time, both output diodes conduct, the transformer secondary voltage drops to zero, and no energy is transferred to the secondary side. The output inductors continue discharging. Mode 5 is depicted in Figure 3.6.

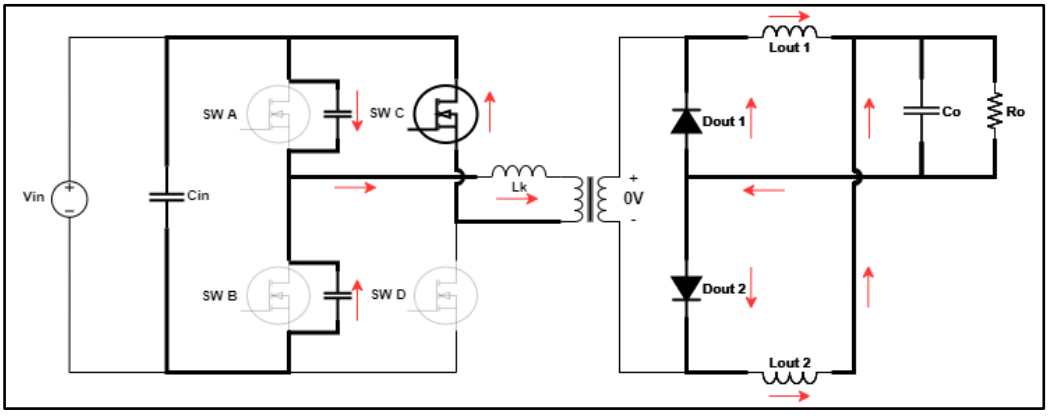

Figure 3.6. PSFB mode 5 (t4 – t5)

3.6. Mode 6 (t5 – t6)

At t5, switch B turns on with ZVS. Similar to Mode 1, the transformer secondary voltage remains zero, and the output diodes conduct while the output inductors discharge. The primary current reverses direction, and no energy is transferred from the primary side until the leakage inductance current reaches the reflected output inductor current. This is another "Duty Cycle Loss Mode", as shown in Figure 3.7.

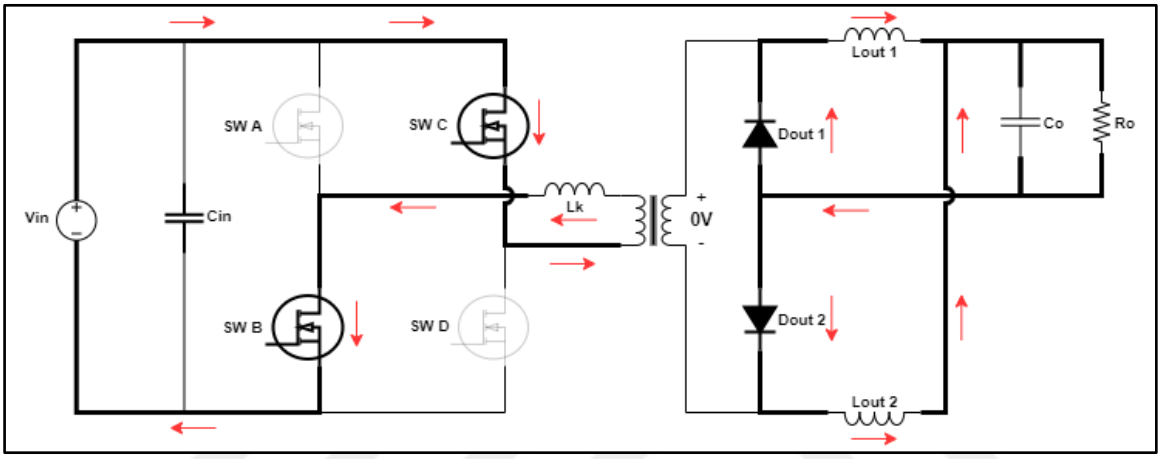

Figure 3.7. PSFB mode 6 (t5 – t6)

3.7. Mode 7 (t6 – t7)

At t6, the transformer secondary voltage increases to the input voltage multiplied by the transformer turns ratio, resuming power delivery to the load. Inductor Lout 2 begins charging, while Lout 1 discharges. Current flows through Dout 1, transferring energy to the output. The effective phase shift begins for the second time in this mode. The current waveform for Mode 7 is shown in Figure 3.8.

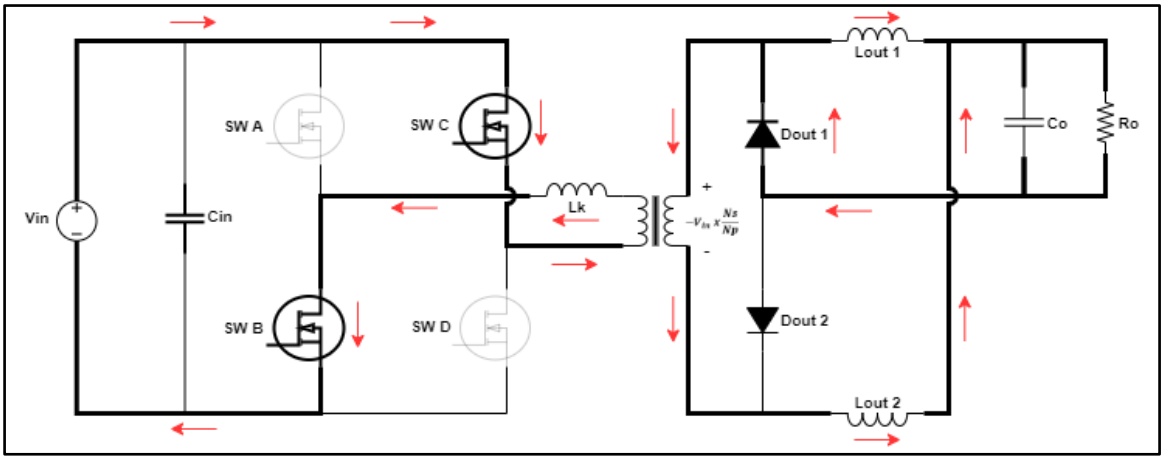

Figure 3.8. PSFB mode 7 (t6 – t7)

3.8. Mode 8 (t7 – t8)

At t7, switch C turns off, and the primary current charges the capacitance of switch C while discharging the capacitance of switch D. This interval, known as the dead time between switches C and D, is necessary for switch D to achieve ZVS by fully discharging its parasitic capacitance. During this period, both output diodes remain conducting, the transformer secondary voltage drops to zero, and no energy is transferred from the primary side to the secondary side. The output inductors continue to discharge. Mode 8 is illustrated in Figure 3.9.

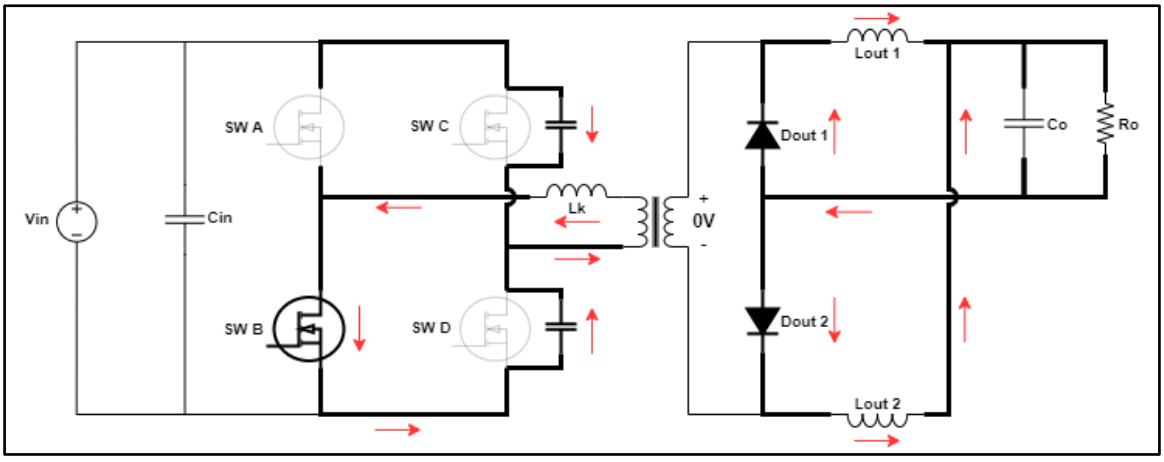

Figure 3.9. PSFB mode 8 (t7 – t8)

3.9. Mode 9 (t8 – t9)

At t8, switch D turns on with ZVS, allowing the primary current to freewheel through switches B and D. No energy is transferred from the primary to the secondary side, as the transformer secondary voltage remains zero. Inductors Lout 1 and Lout 2 discharge through Dout 1 and Dout 2, respectively. Mode 9 is depicted in Figure 3.10.

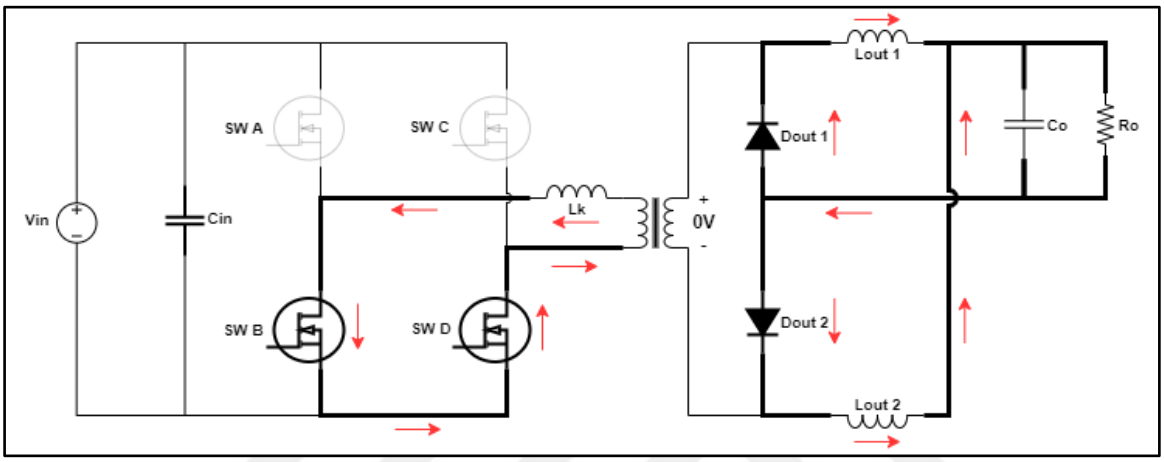

Figure 3.10. PSFB mode 9 (t8 – t9)

3.10. Mode 10 (t9 – t10)

The final mode in one switching cycle begins at t9 when switch B turns off, causing the primary current to charge the capacitance of switch B while discharging that of switch A. This dead time between switches B and A is critical for switch A to achieve ZVS, requiring its parasitic capacitance to fully discharge. During this time, both output diodes conduct, the transformer secondary voltage remains zero, and no energy is transferred to the secondary side. The output inductors continue discharging. Mode 10 is illustrated in Figure 3.11.

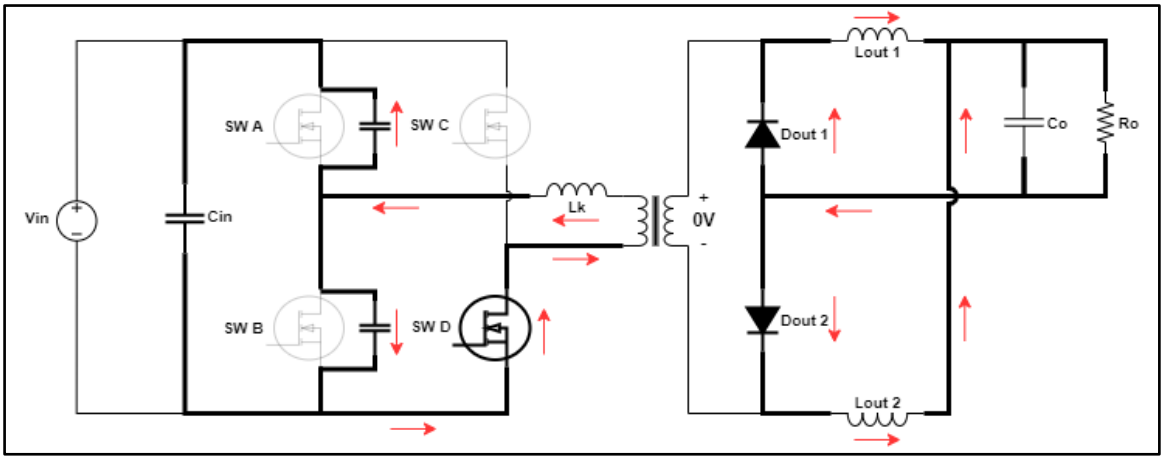

Figure 3.11. PSFB mode 10 (t9 – t10)

4. POWER STAGE DESIGN

Power stage design is an important part of the PSFB converter, and its design has a major impact on performance, efficiency, and ability to meet design specifications [12]. As mentioned in the introduction, this work aims to design a PSFB converter. Input voltage, output voltage, switching frequency and output power were given in the introduction section. All parameters for power stage design are presented in the table below. This section focuses on the selection of components, implementation of ZVS, and verification of the power stage through simulations.

Table 4.1. Design Parameters

Output Power (P_o)	500W
Input Voltage (V_{in})	200V – 400V
Output Voltage (V_o)	28V
Maximum Output Voltage Ripple (ΔV_o)	%0.1
Maximum Output Voltage Overshoot	%10
Maximum Output Inductor Current Ripple (ΔIL_o)	%20
Switching Frequency (f_{sw})	500kHz

4.1. Component Selection

This section details the selection of key components, including the transformer, switches (GaN MOSFETs), rectifier diodes, capacitors, and inductors, with relevant design formulas provided.

4.1.1. Transformer design

The transformer plays a vital role in the PSFB converter by providing electrical isolation and adjusting the voltage between the primary and secondary sides. In addition, Leakage inductance is an inevitable but critical aspect of transformer design in PSFB converters. While leakage inductance is generally considered undesirable in most transformer applications, in a PSFB converter, it can be beneficial as it contributes to the resonant energy required for ZVS [6]. Also, magnetizing inductance represents the inductance due to the magnetization of the core itself. It is primarily responsible for the energy storage in the core and defines the magnetizing current. In a PSFB converter, the magnetizing inductance must

be sufficiently high to limit the magnetizing current, which can contribute to unnecessary circulating losses.

Transformer turn ratio

The turns ratio of the transformer is determined based on the input and output voltage requirements. It directly influences the voltage transformation between the primary and secondary windings. Due to leakage inductance charge time and dead time, effective value off phase shift will be lower than real phase shift. The maximum value of effective phase shift (Pheffmax) was chosen 0.3 to determine turn ratio of transformer.

$$\frac{N_p}{N_s} = \frac{V_{in_{min}}\, Ph_{eff_{max}}}{V_o} \tag{4.1}$$

$$\frac{N_p}{N_s} = \frac{200 \text{ x } 0.30}{28} = 2.14 \approx 2 \tag{4.2}$$

Because of transformer turn ratio is equal to 2, maximum effective phase shift:

$$Ph_{eff_{max}} = 2 \text{ x } \frac{28}{200} = 0.28 \tag{4.3}$$

Leakage inductance of transformer

Leakage inductance is a byproduct of imperfect magnetic coupling between the primary and secondary windings of the transformer [13].

Leakage inductance helps store energy during switching transitions. It enables the ZVS by charging and discharging the parasitic capacitances of MOSFETs with the energy it stores. However, excessive leakage inductance can lead to other challenges, such as voltage overshoots and increased circulating currents [14]. Therefore, leakage inductance must be carefully controlled and optimized. Maximum leakage inductance value depends on the output power, minimum input voltage, turn ratio of transformer, maximum phase shift and frequency.

$$lk_{max} = V_{in_{min}} x \frac{\frac{N_s}{N_p} x\, ph_{max} - \frac{V_o}{V_{in_{min}}}}{\frac{P_o}{V_o} x \left(\frac{N_s}{N_p}\right)^2 x\, f} \quad (4.4)$$

$$lk_{max} = 200 x \frac{0.5 x 0.45 - \frac{28}{200}}{\frac{500}{28} x (0.5)^2 x 500 x 10^3} = 7.6uH \quad (4.5)$$

Considering the diode forward voltage and other losses, the leakage inductance was determined to be 6.5uH.

Magnetizing inductance of transformer

In a PSFB converter, the magnetizing inductance is responsible for creating the magnetizing current in the transformer. It stores energy in the core and helps support the ZVS. High magnetizing inductance reduces magnetizing current and minimizes circulating losses, which can improve efficiency, especially at high power [15]. However, this may result in insufficient energy for ZVS at lighter loads.

Magnetizing inductance value depends on primary MOSFET's output capacitance value. It will be detailed "Achieving Zero Voltage Switching" section of this study.

4.1.2. Selection of MOSFET

GaN MOSFETs are characterized by their high electron mobility, low on state resistance (RDSon), and high breakdown voltage. They provide faster switching speeds and reduced energy losses. They are essential for the 500 kHz switching frequency of the PSFB converter. The selection criteria for GaN MOSFETs include the drain-source voltage rating (VDS), current rating (ID), and RDSon in this study.

The voltage rating should be higher than the maximum input voltage with a safety margin.

$$V_{DS} > V_{in_{max}} x \text{ Safety Factor} \quad (4.6)$$

Maximum input voltage for this study is 400V and safety factor is 1.5. VDS should be more than 600V.

The maximum current rating is based on the output power, output voltage and turn ratio of transformer. Following equation shows the MOSFET RMS current calculation in PSFB.

$$I_{rms_{mosfet}} = \frac{P_o}{V_o} \text{ x } \frac{1}{2} \text{ x } \frac{N_s}{N_p} \text{ x } \sqrt{\frac{1}{2}} \tag{4.7}$$

$$I_{rms_{mosfet}} = \frac{500}{28} \text{ x } \frac{1}{2} \text{ x } \frac{1}{2} \text{ x } \sqrt{\frac{1}{2}} = 3.15A \tag{4.8}$$

RDSon causes conduction loss. When choosing the MOSFET, it was decided that the conduction loss should be below 1W. ZVS is used in PSFB converters to minimize switching losses during the turn-on phase of MOSFETs. However, even with ZVS, there are still some switching losses, especially during the turn-off transition and it leads to extra power loss. Considering that the MOSFETs in this study will operate without an external cooling system, minimizing conduction losses was prioritized in the selection process.

$$P_{conduction} = I^2_{rms_{mosfet}} \text{ x } R_{DSon} \tag{4.9}$$

$$R_{DSon} \leq \frac{1}{3.15^2} = 0.1\Omega \tag{4.10}$$

Based on these criteria, the MOSFET with manufacturer number GS-065-018-2-L from GaN Systems was selected.

4.1.3. Selection of output diodes

The output diodes in a Current Doubler Rectifier are important for converting the high-frequency AC output from the transformer to DC. The key parameters in selecting the output diodes include the reverse voltage (Vr), maximum current rating (If) and forward voltage drop (Vf).

Output diodes should withstand the seconder side voltage of transformer. Reverse voltage should be higher than the maximum input voltage with a safety margin.

$$V_{r_{max}} > V_{in_{max}} \text{ x } \frac{N_s}{N_p} \text{ x safety factor} \tag{4.11}$$

$$V_{r_{max}} > 400 \text{ x } 0.5 \text{ x } 1.5 = 300V \tag{4.12}$$

Reverse voltage of diode should be more than 300V.

RMS current of diodes depends on the output current and effective phase shift.

$$I_{D_{rms\ max}} = \frac{P_o}{V_o} \text{ x } \sqrt{\frac{ph_{eff_{max}}}{2} + \frac{1}{4}} \tag{4.13}$$

$$I_{D_{rms\ max}} = \frac{500}{28} \text{ x } \sqrt{\frac{0.28}{2} + \frac{1}{4}} = 11.15A \tag{4.14}$$

To minimize conduction losses, diodes with a low forward voltage drop are essential. Additionally, high-speed recovery diodes are preferred to reduce switching losses and EMI. Considering the high current levels expected in the rectifier, Schottky diodes are preferred due to their low forward voltage and fast switching characteristics.

Taking these factors into account, the diode with part number SBR40U300CTB was selected. These diodes are well suited for the high-frequency operation of the PSFB converter, minimizing losses and contributing to the overall efficiency of the system. However, despite being one of the most efficient diodes available on the market, the lack of active cooling in the design means that the power consumption in each diode will still be significant. To alleviate this, 2 diodes will be used in parallel to reduce the loss per diode, ensuring that thermal limits are not exceeded and increasing system reliability.

4.1.4. Output inductors

The design of the output filter is critical to reduce output ripple and maintain stable operation. The selection of the output inductor based on current rating and current ripple of inductor. Output inductor average current depends on output power and output voltage.

$$I_{L_{out}(avg)} = \frac{P_o}{2V_o} \tag{4.15}$$

$$I_{L_{out}(avg)} = \frac{500}{2 \text{ x } 28} = 8.92 \tag{4.16}$$

The worst case ripple was determined as a %20 of inductor current. It occurs when input is maximum.

$$L_{out} > \frac{\left(V_{in_{max}} \frac{N_s}{N_p} - V_o\right)}{\Delta I_{L_{out}} \ fs} \frac{N_p}{N_s} \frac{V_o}{V_{in_{max}}} \tag{4.17}$$

$$L_{out} > \frac{(400 \text{ x } 0.5 - 28)}{8.92 \text{ x } 0.2 \text{ x } 500k} \text{x } 2 \text{ x } \frac{28}{400} = 26.9uH \tag{4.18}$$

Output inductance was determined as a 30uH.

4.1.5. Output capacitor

The output capacitor is crucial for smoothing the rectified output and providing a stable DC voltage to the load. In this study, the selection criteria for the output capacitor include voltage rating and peak overshoot specification of converter.
The voltage rating should be higher than the maximum output voltage with a safety margin:

$$V_{capacitor} > V_{out} \text{ x Safety Factor} \tag{4.19}$$

Output voltage for this study is 28V and safety factor is 1.5. Capacitor rated voltage should be more than 42V.

When the load is suddenly removed, the voltage at the output overshoots. To limit amount of overshoot, the capacitance is selected according to following equation.

$$C_o \geq \frac{L_{out} \text{ x } I^2_{L_{outmax}}}{kV_o^2 - V_o^2} \tag{4.20}$$

Where k is the overshoot factor. In this study maximum overshoot value was accepted %10 of output voltage.

$$C_o \geq \frac{30 \text{ x } 10^{-6} \text{ x } (8.92 \text{ x } 1.1)^2}{1.1 \text{ x } (28^2) - (28^2)} = 36.8\text{uF} \tag{4.21}$$

Output capacitance was determined as a 47uF. After selection of capacitance value, the worst-case output voltage ripple was checked. When input voltage is maximum, the worst-case output voltage occurs. Ripple value below %0.1 of the output voltage was accepted in this study.

$$\Delta V_o = \frac{Vo \text{ x} \left(1 - 2\frac{N_p}{N_s}\frac{V_o}{V_{in_{max}}}\right)}{16 \, L_o \, C_o \, fs^2} \tag{4.22}$$

$$\Delta V_o = \frac{28 \text{ x } \left(1 - 2\frac{2}{1}\frac{28}{400}\right)}{16 \text{ x } 30 \text{ x } 10^{-6} \text{ x } 47 \text{ x } 10^{-6} \text{ x } (500 \text{ x } 10^3)^2} = 3.5\text{mV} \tag{4.23}$$

In military applications, particularly in high-altitude environments, electrolytic capacitors are generally not preferred due to their decreased reliability and performance at low pressure and low temperature conditions. Instead, ceramic capacitors are chosen for their robustness and stability in such extreme environments. Ceramic capacitors also offer low ESR and high ripple current capabilities, making them well-suited for high-frequency, high-reliability applications like the PSFB converter. To achieve the required capacitance value, multiple ceramic capacitors can be used in parallel, allowing for both increased capacitance and

improved current-handling capacity. This also helps distribute the heat generated during operation, further enhancing reliability.

4.2. Achieving Zero Voltage Switching

ZVS is a very important aspect in PSFB converters, especially to minimize switching losses and increase overall efficiency. In ZVS, MOSFETs are turned on when the voltage across them is zero, thus eliminating the overlap of voltage and current during switching transitions.

4.2.1. Energy requirements for ZVS

To achieve ZVS in PSFB converter, it is necessary to have sufficient energy stored in the circuit's parasitic elements, such as the leakage inductance and magnetizing inductance of the transformer. This stored energy is used to charge and discharge the MOSFETs' output capacitance during the switching transitions. Under no-load and light-load conditions, ZVS might not be achieved if the circuit lacks enough inductive energy to adequately charge and discharge the output capacitance of the two FETs in the same bridge leg.

As seen in Figure 2.6, there are four switches on the input side of the converter. The energy stored in transformer parasitics is greater for switches A and B than for switches C and D [6]. This results in a broader ZVS range for switches C and D compared to A and B. The total capacitive energy is the same for all mosfet and is given following equation. Transformer capacitance is ignored on this study.

$$E_c \approx C_{o(er)} \times V_{in}^2 \tag{4.24}$$

Co(er) is the fixed capacitance that would give the same stored energy as Coss while VDS is rising from 0V to the stated VDS. This value is shared in datasheet. Figure 4.1 shows the datasheet information.

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V, I_{DSS} ≤ 35 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		78	110	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 5.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		197		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 5.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 4.8 mA
Gate-to-Source Current	I_{GS}		110		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.5		V	V_{DS} = 400 V, I_{DS} = 18 A
Drain-to-Source Leakage Current	I_{DSS}		1.2	35	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		42		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		1.3		Ω	f = 5 MHz, open drain
Input Capacitance	C_{ISS}		132		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		34		pF	
Reverse Transfer Capacitance	C_{RSS}		0.4		pF	
Effective Output Capacitance Energy Related (Note 4)	$C_{O(ER)}$		58		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related (Note 5)	$C_{O(TR)}$		90		pF|	
Total Gate Charge	Q_G		4		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		1.2		nC	
Gate-to-Drain Charge	Q_{GD}		1.2		nC	
Output Charge	Q_{OSS}		37		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

Figure 4.1. Datasheet information for GS-065-018-2-L

To obtain ZVS, inductive energy should be bigger than capacitive energy.

$$E_{c_{max}} \approx 58\text{pF x } 400^2 \approx 9.2\text{uJ} \tag{4.25}$$

Inductive energy for A and B switches

In the PSFB converter, only the leakage inductance contributes to the ZVS. Therefore, the ZVS range narrower for these switches.

$$E_{L_{swA,B}} = 0.5\, l_k \left(I_{magnetizing_{peak}} + I_{Lout_{min}} \frac{N_s}{N_p} \right)^2 \tag{4.26}$$

Although only leakage inductance energy contributes, the magnetizing current peak value also affects the total amount of energy. This is directly related to the magnetizing inductance value.

$$I_{magnetizing_{peak}} \approx \frac{1}{2} \text{ x} \frac{V_{in}}{L_{magnetizing}} \text{ x } \frac{ph}{f} \tag{4.27}$$

By substituting “Eq. 4.27” into equation “Eq. 4.26”, the magnetizing inductance value can be obtained, illustrating its impact on the total energy and, consequently, on the ZVS operation.

$$L_{magnetizing} \approx \frac{\frac{1}{2} \text{ x } V_{in} \text{ x} \frac{ph}{f}}{\sqrt{\frac{E_{L_{swA,B}} \text{ x } 2}{l_k}} - I_{Lout_{min}} \frac{N_s}{N_p}} \tag{4.28}$$

To calculate the magnetizing inductance, the minimum current of the output inductor was determined, with the assumption that the converter operates in continuous conduction mode. At an output power of 200W, the minimum current of the output inductor is calculated to be approximately 3.1A, with a corresponding phase shift of around 0.17. Based on these conditions, and to ensure sufficient energy for ZVS operation, the magnetizing inductance is determined to be approximately 500µH.

$$L_{magnetizing} \approx \frac{\frac{1}{2} \text{ x } 400 \text{ x} \frac{0.17}{500 \text{ x } 10^3}}{\sqrt{\frac{9.2 \text{ x } 10^{-6} \text{ x } 2}{6.5 \text{ x } 10^{-6}}} - 3.1 \text{ x} \frac{1}{2}} = 500\text{uH} \tag{4.29}$$

<u>Inductive energy for C and D switches</u>

The energy contributions come from the leakage inductance, magnetizing inductance and the reflected output inductor. As a result, the ZVS range for switches C and D is broader compared to that of switches A and B.

$$E_{L_{swC,D}} = 0.5L_{magnetizing}I^2_{magnetizing_{peak}} + 0.5L_{out}\left(\frac{N_p}{N_s}\right)^2\left(I_{Lout_{max}}\frac{N_s}{N_p}\right)^2 + 0.5L_K\left(I_{Mpk} + I_{Lout_{max}}\frac{N_s}{N_p}\right)^2 \tag{4.30}$$

4.2.2. Deadtime calculation

The deadtime is the period during which both the high-side and low-side MOSFETs of a leg in the full-bridge are turned off, allowing the ZVS condition to be met. Properly calculating the deadtime is critical for ensuring reliable ZVS operation [16]. If the deadtime is too short, ZVS may not be fully achieved. Conversely, if the deadtime is too long, it can reduce the efficiency of the converter and introduce voltage spikes. The deadtime can be calculated based on the time required for the leakage inductance to discharge the MOSFETs' output capacitance.

$$\text{Deadtime} \geq \frac{\pi}{2}\sqrt{L_K \text{ x } \left(2 \text{ x } C_{o(tr)}\right)} \tag{4.31}$$

Co(tr) is the fixed capacitance that would give the same charging time as Coss while VDS is rising from 0 V to the stated VDS.

$$\text{Deadtime} \geq \frac{\pi}{2}\sqrt{6.5 \text{ x } 10^{-6} \text{ x } (2 \text{ x } 90 \text{ x } 10^{-12})} = 54\text{ns} \tag{4.32}$$

4.3. Verification of Power Stage with Simulation

To validate the power stage design of the PSFB converter, detailed simulations were performed using both LTspice and PLECS. These simulations were used to analyze the circuit's performance ensuring compliance with the design specifications outlined in Table 4.1. Key parameters, including output voltage (V_o), output voltage ripple (ΔV_o), inductor current ripple (ΔIL_o), MOSFET current, diode current, and the system's response to load transients, were thoroughly examined.

4.3.1. LTspice simulations

With the LTspice simulations were particularly focused on utilizing original device models provided by manufacturers, ensuring the most accurate representation of the real-world behavior of the components. This approach allows for precise evaluation of electrical characteristics, such as switching transitions and conduction losses, under realistic operating

conditions. The PSFB converter's circuit schematic was developed in LTspice presented in Figure 4.2.

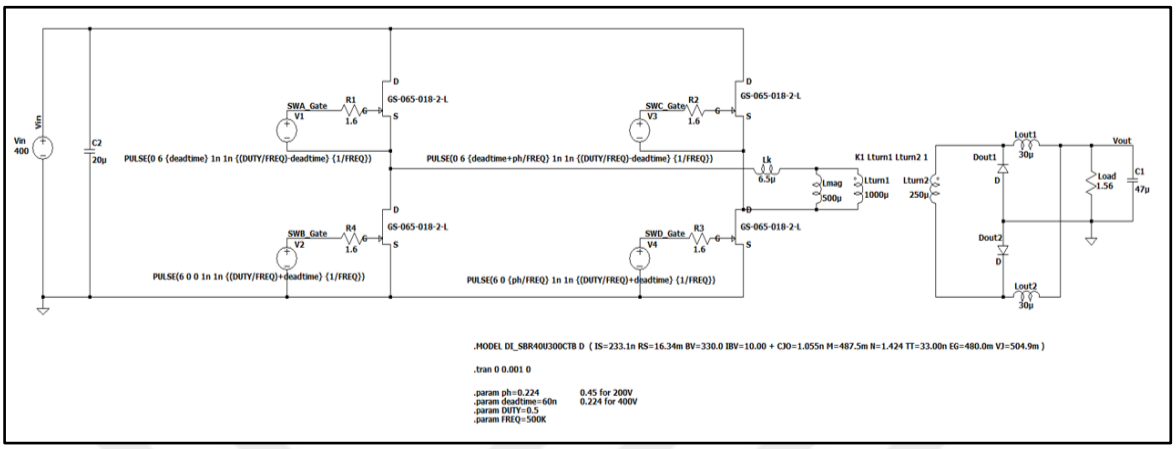

Figure 4.2. PSFB circuit schematic on LTspice

The gate signals applied to the MOSFETs were carefully designed to ensure proper timing and ZVS operation. These signals were simulated in LTspice and verified to meet the required phase-shift modulation strategy. The signals for switches A, B, C, and D are shown in Figure 4.3. The timing and deadtime between complementary switches were validated to prevent overlap while enabling switching transitions.

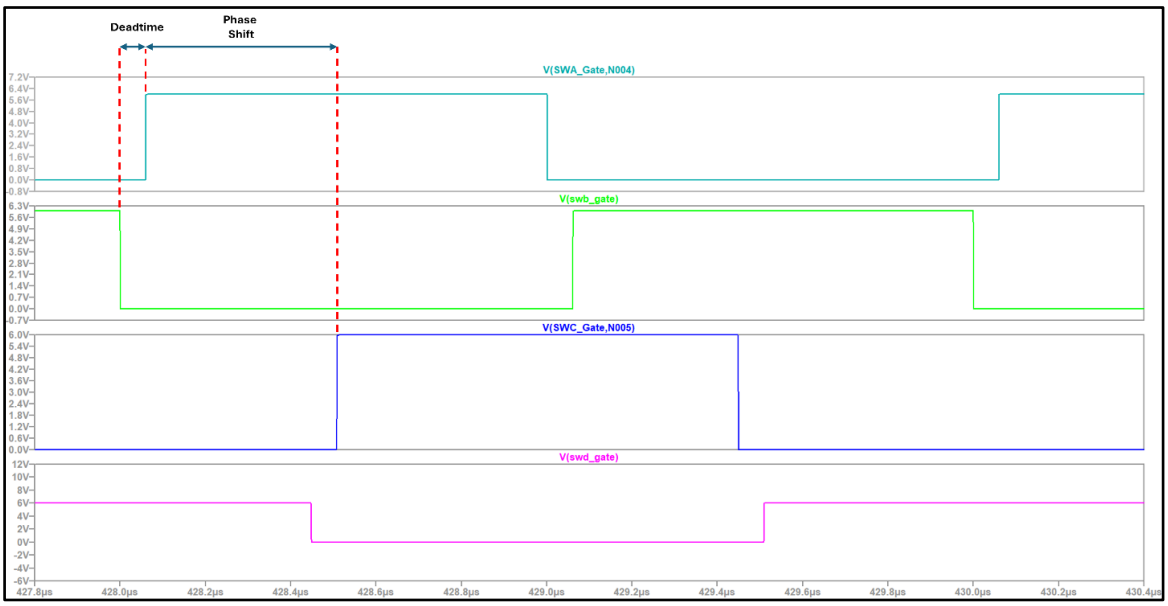

Figure 4.3. Gate signals on LTspice

Output voltage and power performance

The output voltage was simulated under the full input voltage range (200–400V) to ensure stable regulation at 28V, as required. Figure 4.4 and Figure 4.5 illustrate the steady-state output voltage waveforms at input voltages of 200V and 400V, respectively. The output power was also verified to be 500W under full load conditions, meeting the design specifications.

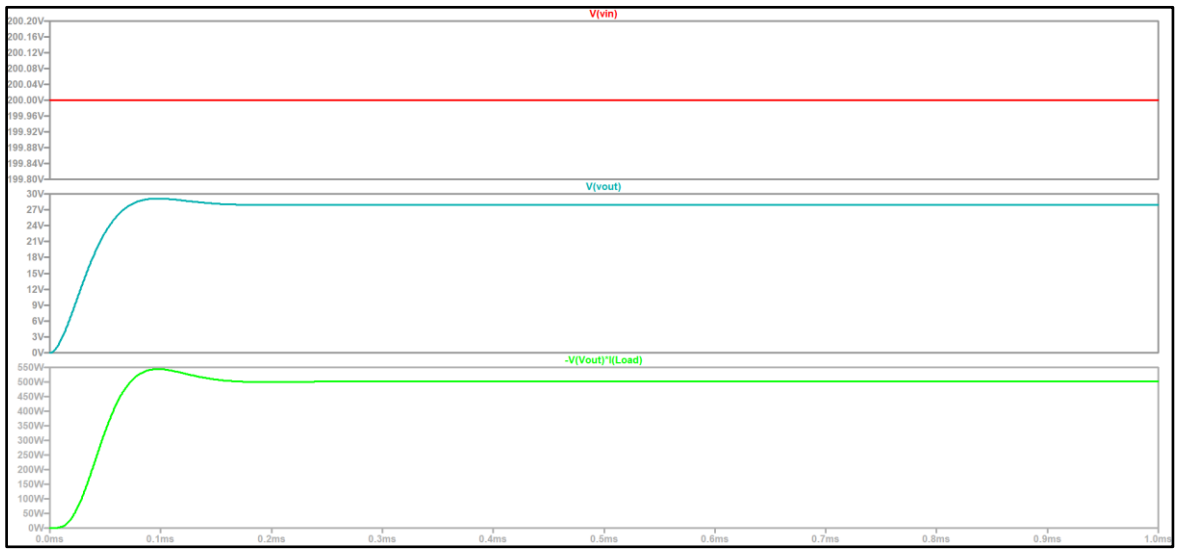

Figure 4.4. Output voltage and power waveforms at 200V input voltage

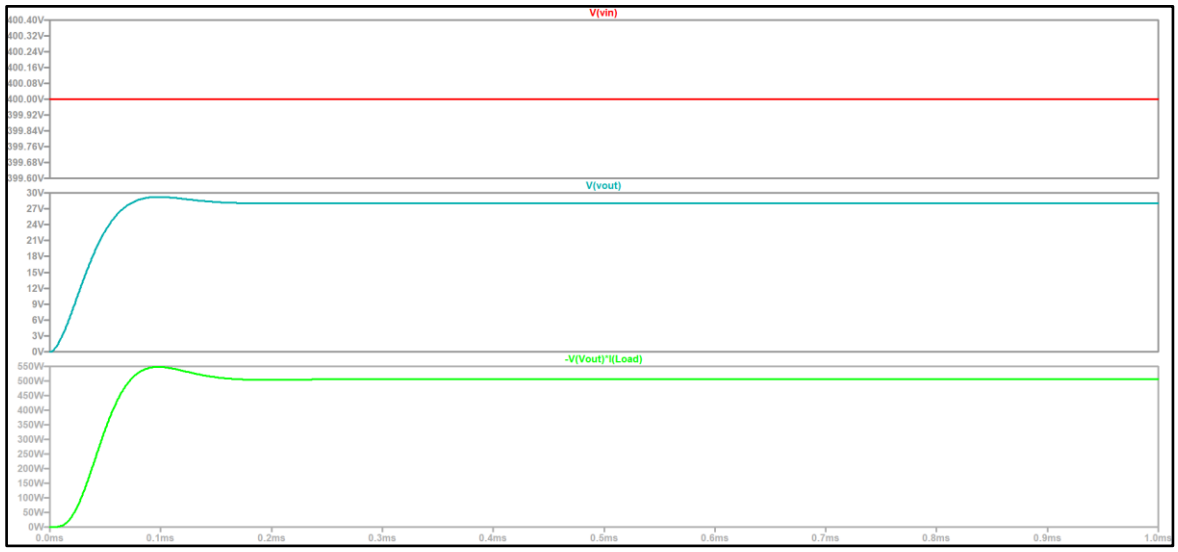

Figure 4.5. Output voltage and power waveforms at 400V input voltage

Output voltage ripple

The output voltage ripple was simulated at the maximum input voltage of 400V, as this represents the worst-case scenario. The results showed a ripple of less than 0.1%, which complies with the design criteria. Figure 4.6 presents the output voltage ripple waveform.

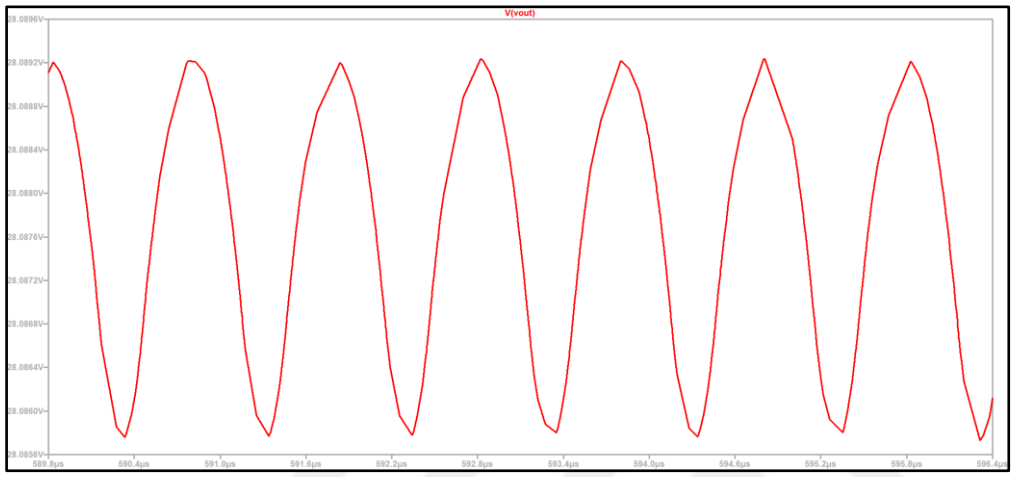

Figure 4.6. Output voltage ripple

Inductor current ripple

The inductor current ripple was analyzed for the two output inductors. At maximum load and input voltage, the ripple was found to be within the specified 20% of the average inductor current. Figure 4.7 displays the inductor current ripple waveforms, validating the correct selection of output inductance.

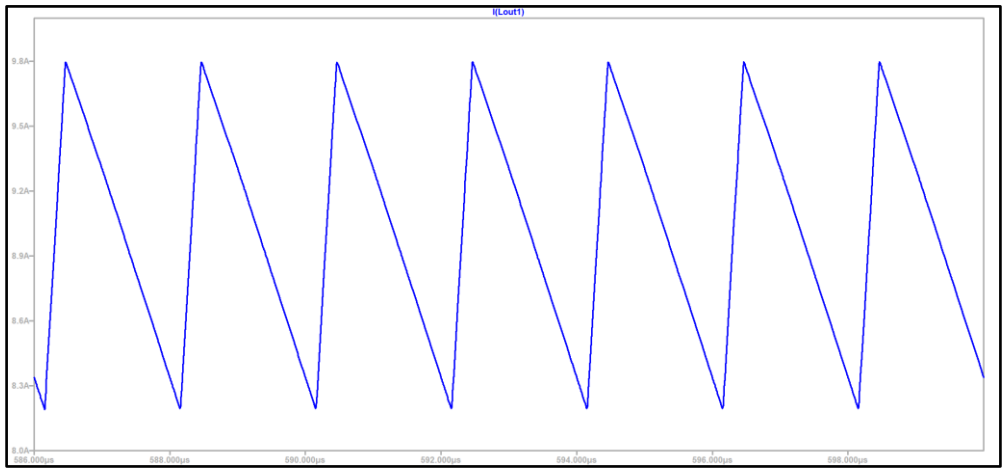

Figure 4.7. Inductor current ripple

MOSFET and diode currents

The currents through the MOSFETs and output diodes were analyzed to verify the accuracy of the calculations and assess the suitability of the selected components. The current waveforms for the primary MOSFETs, shown in Figure 4.8, align with the calculated RMS current values, confirming the design assumptions.

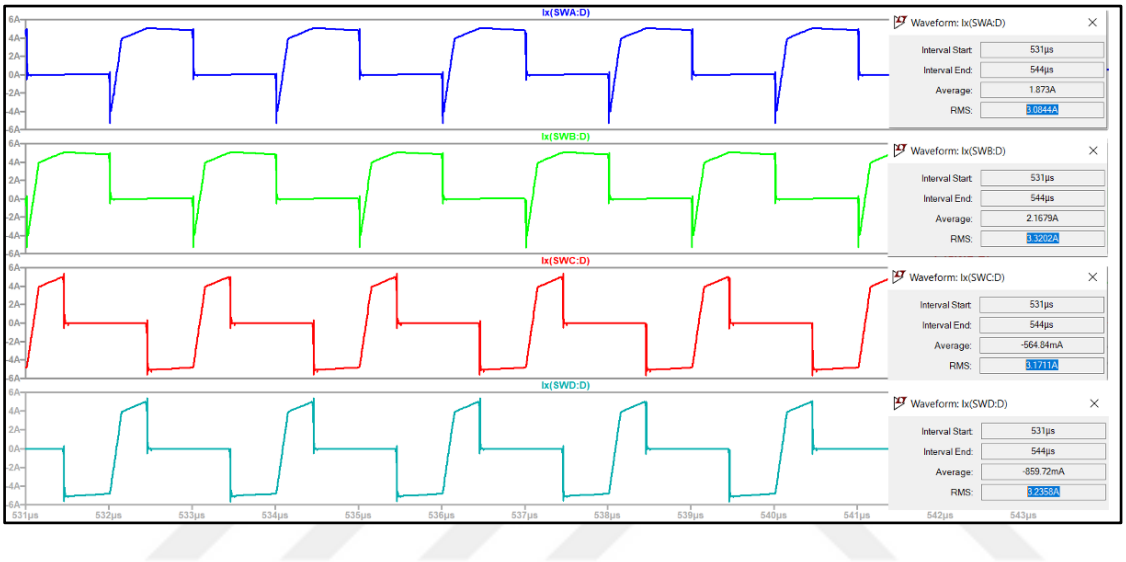

Figure 4.8. MOSFET's current waveforms

Similarly, the diode current waveforms, illustrated in Figure 4.9, validate the calculated current ratings. These waveforms also demonstrate smooth conduction with minimal reverse recovery effects.

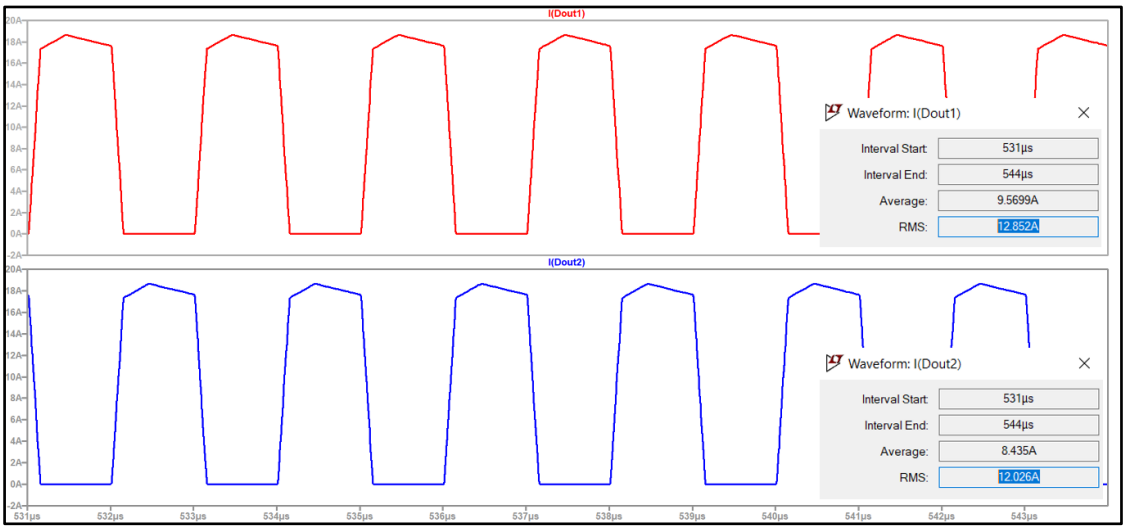

Figure 4.9. Diode current waveforms

Assestment of ZVS

ZVS is a critical feature of the PSFB converter, enabling the MOSFETs to turn on with minimal switching losses. To evaluate the achievement of ZVS, simulation results for the VDS and gate-source (VGS) voltage of switch A were analyzed. The waveforms for VDS and VGS, presented in Figure 4.10, clearly demonstrate the ZVS operation. The VDS drops to zero before the VGS rises, ensuring that the MOSFET turns on without overlapping voltage and current. This minimizes switching losses. These results validate the effectiveness of the ZVS mechanism in the PSFB converter, confirming the proper design of the transformer leakage inductance, switching timing, and deadtime between complementary switches.

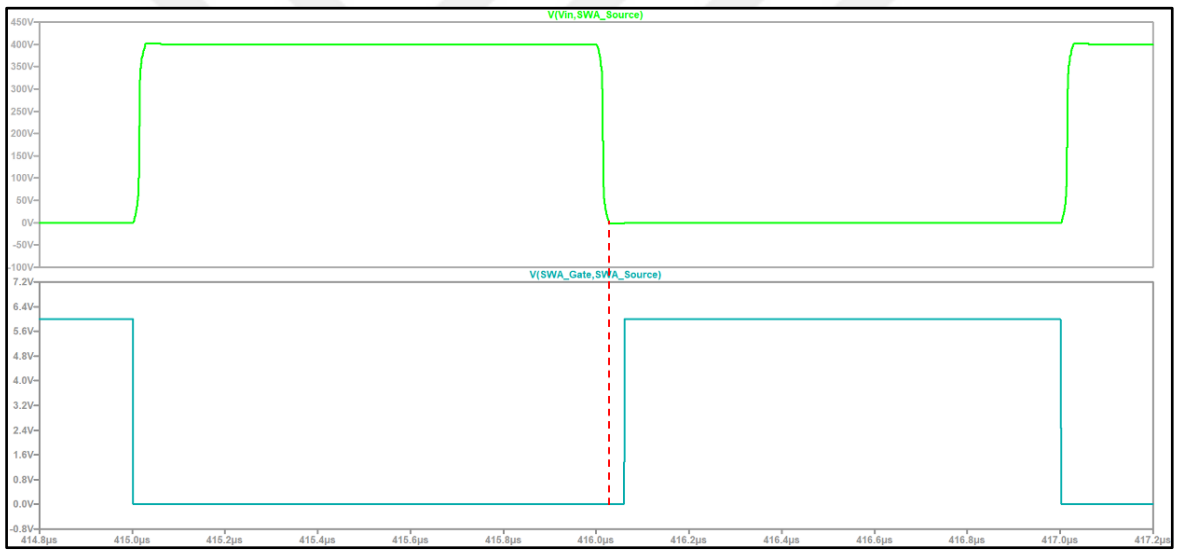

Figure 4.10. VDS and VGS waveforms for switch A

4.3.2. PLECS simulations

In addition to LTspice, PLECS was utilized for system-level simulations of the PSFB converter to validate its performance under various operating conditions. PLECS offers a high-level simulation environment optimized for power electronics and allows for efficient analysis of dynamic behavior. Throughout this study, ideal circuit elements were employed in all PLECS simulations, ensuring a straightforward evaluation of the system's transient and steady-state responses. All simulations performed in LTspice were also replicated in PLECS, yielding consistent results under steady-state conditions.

This section focuses only on the output voltage response during transient load analyzed in PLECS. According to the design specifications outlined in Table 4.1, the output voltage must not deviate by more than 10% of output voltage during sudden load changes. The transient response was evaluated under open-loop control to simulate the worst-case scenario, specifically examining the system's behavior when the load is suddenly removed. If the output voltage overshoot exceeds 10%, closed-loop control would not adequately compensate for the deviation, making proper output capacitor selection critical. The selected capacitor value was verified through simulation, confirming its adequacy in maintaining the voltage within acceptable limits during transients.

The circuit diagram for the scenario where the load is abruptly removed is presented in Figure 4.11, and the corresponding simulation results are shown in Figure 4.12. These results validate the design and confirm the system's ability to meet the transient response criteria.

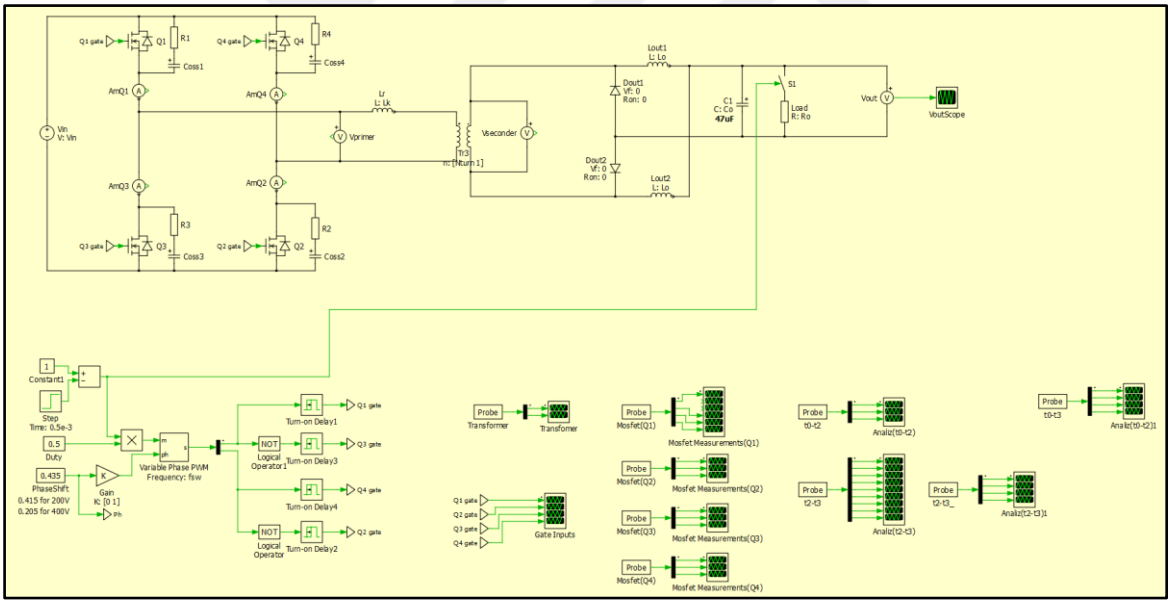

Figure 4.11. Circuit diagram for sudden load removal on PLECS

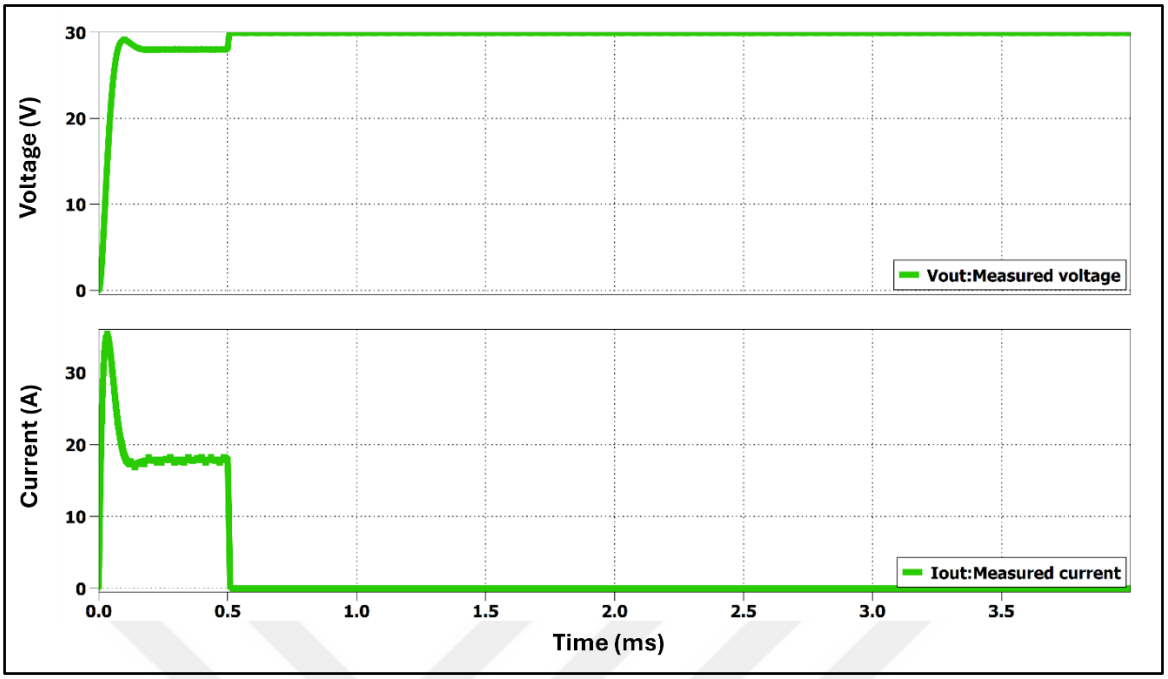

Figure 4.12. Simulation results for load transient response

Both simulation platforms yielded consistent results, validating the accuracy of the design. While LTspice provided detailed time-domain waveforms and insights into individual component behaviors, PLECS enabled fast system-level simulations and efficiency analysis, making it an excellent tool for verifying performance under multiple operating scenarios. The simulation results confirmed the Power stage of PSFB converter's compliance with design requirements. With the power stage successfully verified, the next step focuses on the design of the controller.

5. CONTROLLER DESIGN

A closed-loop controller is essential for maintaining the stability and performance of the system. Figure 5.1 shows the general form of closed loop system for converters.

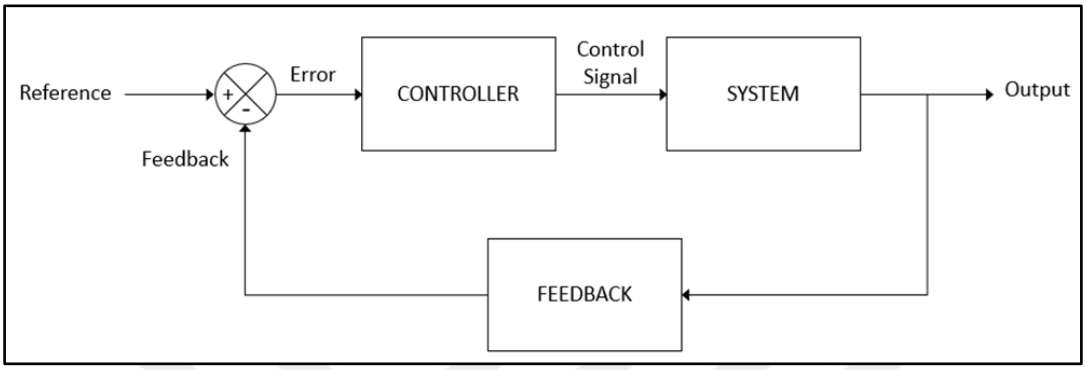

Figure 5.1. General closed-loop system

The primary function of the controller for PSFB is to regulate the output voltage by dynamically adjusting the phase shift between the gate signals of the primary MOSFETs and generate the desired output regardless of the any changes to the parameters. This study intends to design voltage mode-controlled (VMC) and current mode-controlled (CMC) PSFB converter.

5.1. Voltage Mode Control Design of PSFB Converter

VMC architecture uses feedback from the output voltage to adjust the phase shift of the primary-side MOSFETs. A compensator is employed to ensure that the output voltage tracks the reference voltage. Figure 5.2 shows the general form of VMC system for converters.

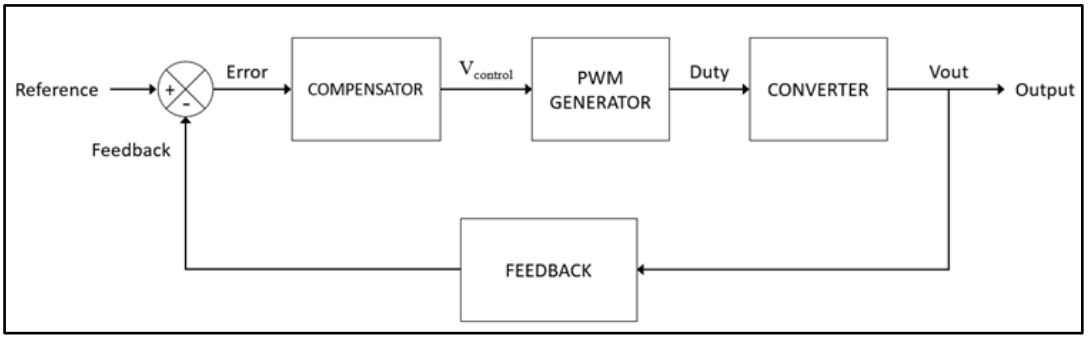

Figure 5.2. General VMC closed loop system diagram

The transfer function of each block of the system in Figure 5.2 must be developed to describe the control properties. Pulse Width Modulation (PWM) generator and Feedback blocks are accepted as a “1” on this study. To make a compensator design, converter transfer function is needed.

5.1.1. Modelling of PSFB converter for VMC

Accurate modeling of the PSFB converter is crucial for developing an effective closed loop controller. The converter model must capture the key dynamics of the converter. Small-signal modeling is often used to analyze the converter's response to changes in input voltage, load, and control inputs. Small-signal models provide insights into the stability and dynamic performance of the converter, which are critical for designing robust control strategies. Several small signal models are presented in the literature for PSFB [17-19]. Small signal model for VMC in [17] was used in this study, but it has been arranged for PSFB Converter with Current Doubler Rectifier.

$$\frac{\tilde{v}_o}{\widetilde{ph}} = \frac{2V_{in}\frac{N_s}{N_p}}{s^2LC + s\left(\frac{L}{R_o} + 2\left(\frac{N_s}{N_p}\right)^2 f_{sw}L_KC\right) + \frac{2\left(\frac{N_s}{N_p}\right)^2 f_{sw}L_K}{R_o} + 2} \tag{5.1}$$

The behavior of the small-signal model was compared with the circuit model using PLECS simulations. Circuit schema is shown in Figure 5.3 and comparison results are shown in Figure 5.4.

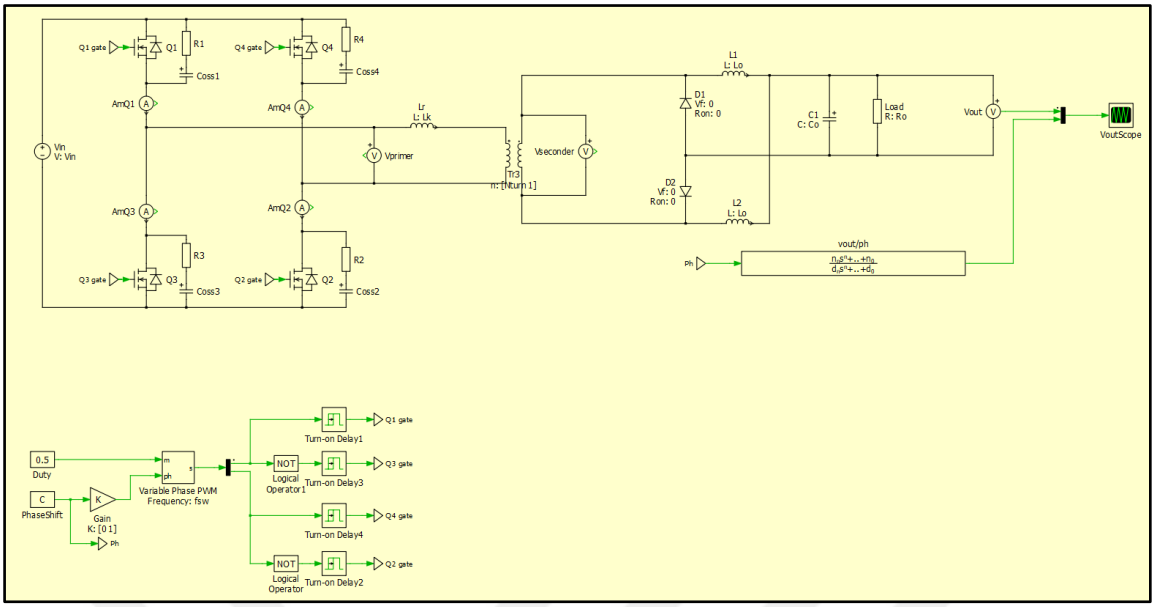

Figure 5.3. PSFB converter schema and transfer function of converter

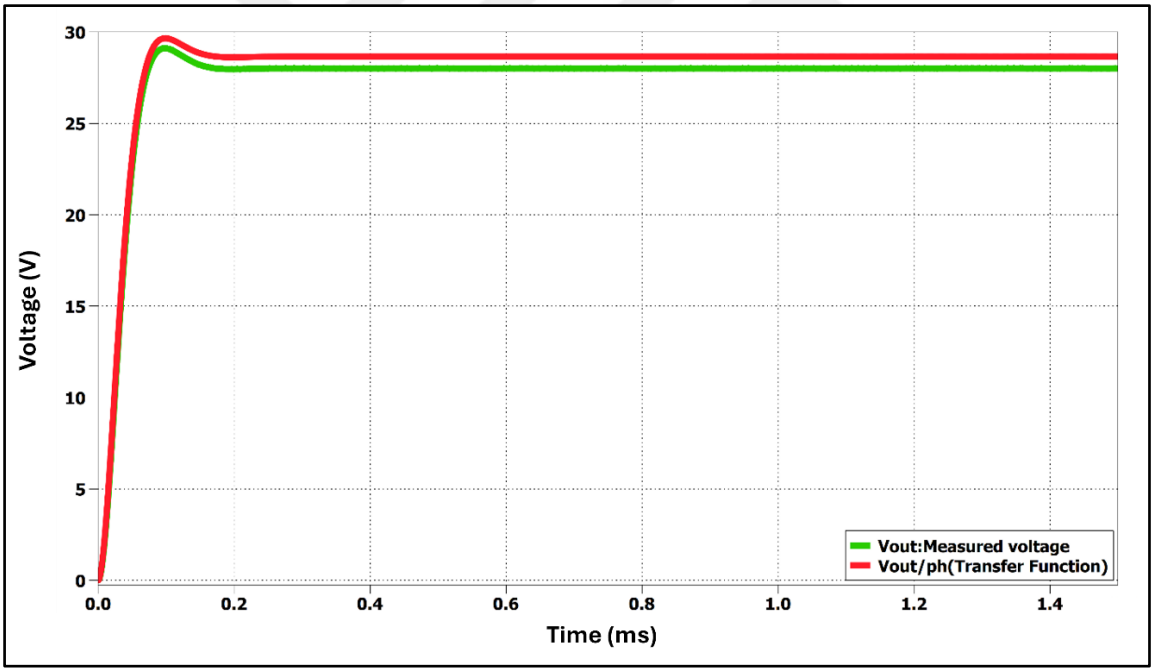

Figure 5.4. Comparison of the result of PSFB converter transfer function (Vout/ph)

The derived transfer function accurately represents the dynamic behavior of the converter.

5.1.2. Compensator design for VMC

Before starting the compensator design, the last situation of closed loop system is given in Figure 5.5.

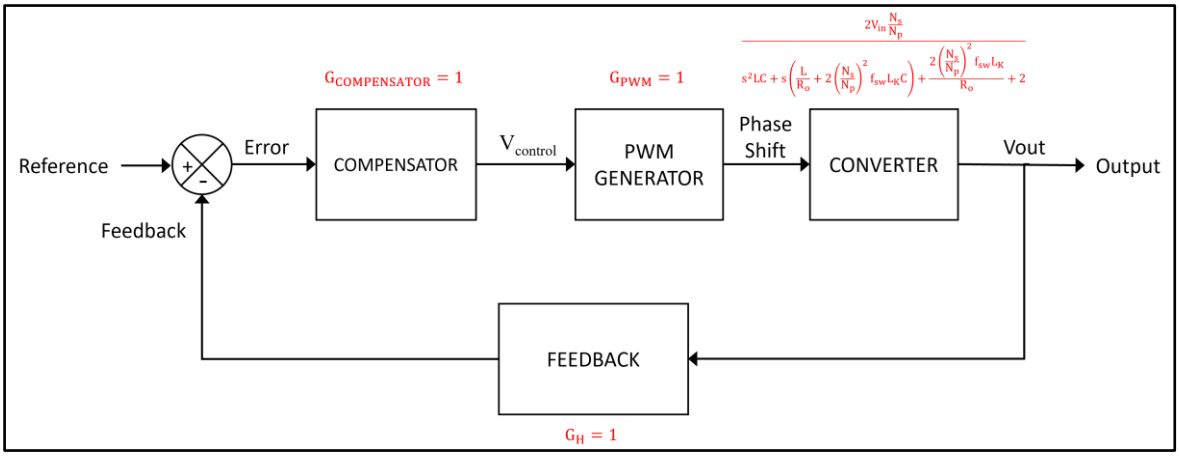

Figure 5.5. Closed-loop system before compensator design

To assess system stability and dynamic performance, the step response of the closed-loop system was analyzed. Step response analysis is an effective tool for evaluating transient behavior, including rise time, settling time, overshoot, and steady-state error, all of which are key indicators of system stability. Figure 5.6 illustrates the configuration used to simulate the step response of the system without compensation. The simulation results, presented in Figure 5.7, reveal the system's response to a step input.

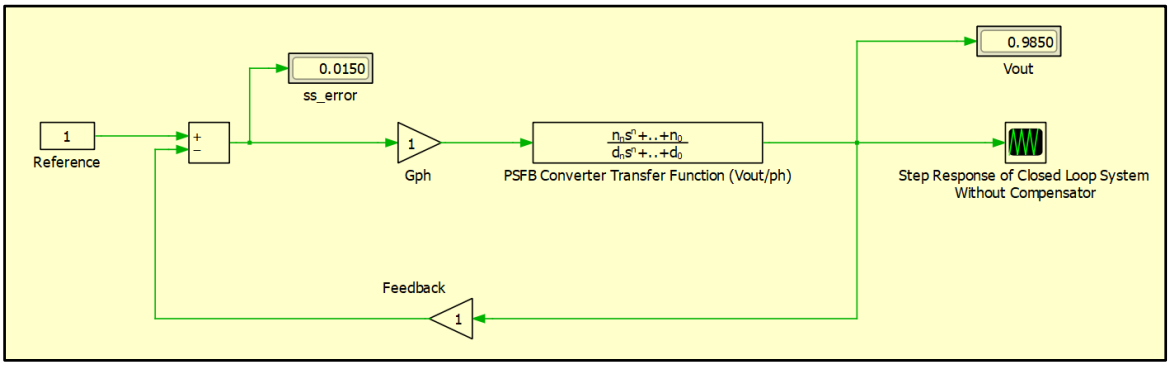

Figure 5.6. Closed-loop system step response schema without compensator

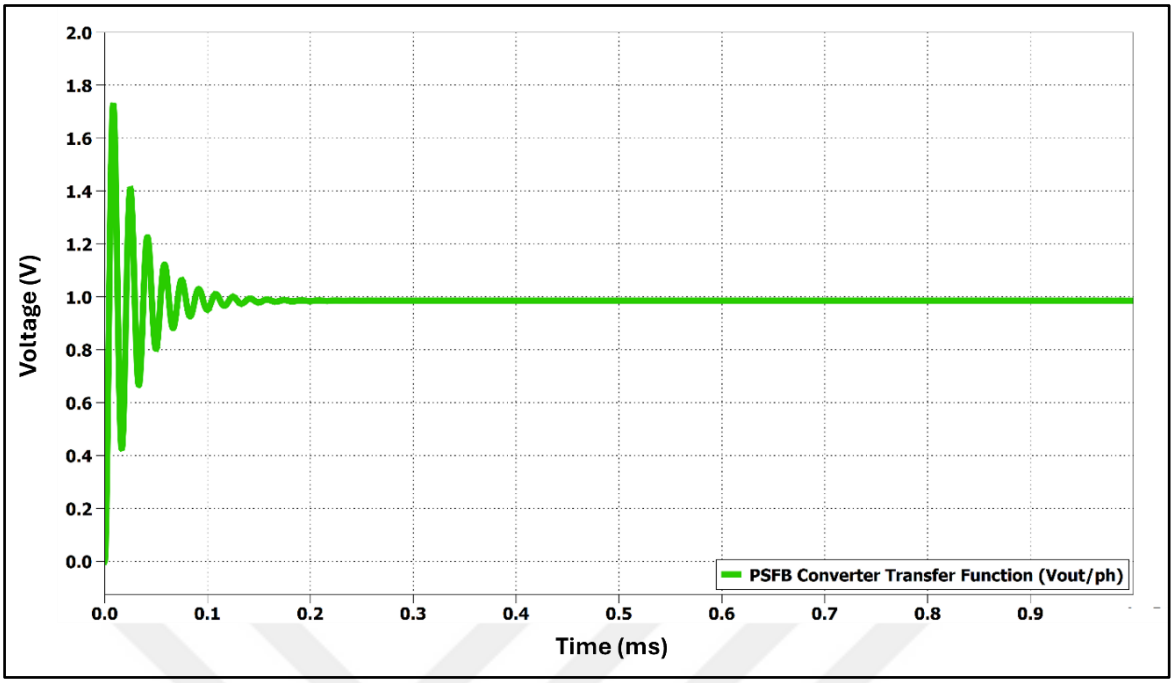

Figure 5.7. Step response without compensator

According to simulation results, the system is unstable and requires compensation to enhance stability, reduce overshoot, and improve transient response.

The compensator design is based on the small-signal model. Compensators are carefully designed to ensure that the closed-loop system exhibits adequate phase margin and crossover frequency, guaranteeing both stability and fast transient response. The performance and stability of the control loop used to regulate the output voltage of a converter can be assessed by analyzing its open-loop characteristics [1]:

1. At low frequencies, a high gain ensures that the steady-state error between the output and the reference signal remains minimal.

2. Normally, a large bandwidth is beneficial for achieving a fast response and minimizing delay in closed-loop systems. However, for converters, the gain at the converter's switching frequency should be small to avoid issues such as instability, noise amplification, and interference with the switching harmonics, which can lead to degraded performance.

3. The phase margin should ideally be between 45° and 90° to ensure stable operation, providing a sufficient buffer to avoid instability while maintaining good dynamic response in the feedback loop.

To determine compensator's characteristic, open loop transfer function is needed and also to find open loop transfer function, closed loop system should be broken after feedback network. Broken closed loop system is shown in Figure 5.8.

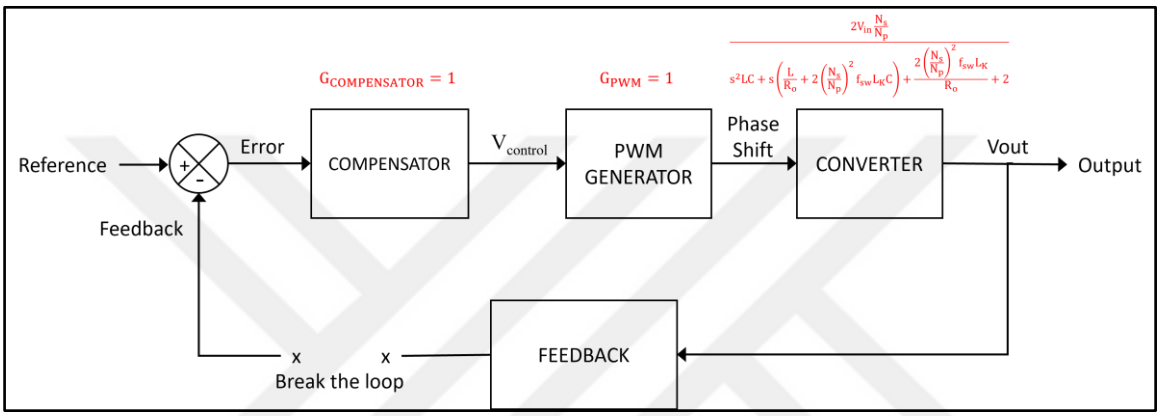

Figure 5.8. Broken closed-loop system for VMC

After break the loop, open loop transfer function is equal to transfer function of converter. Bode plot of open loop transfer function was found with MATLAB and shown in Figure 5.9.

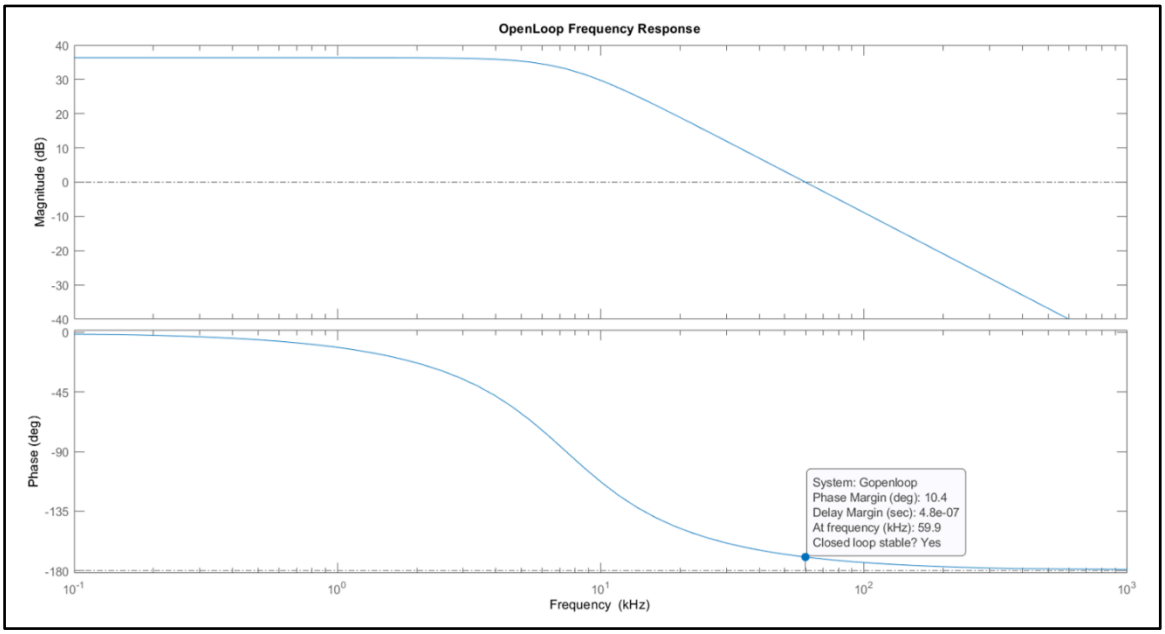

Figure 5.9. Bode plot of open loop transfer function for VMC

The Bode plot in Figure 5.9 reveals that the crossover frequency is approximately 1/8th of the switching frequency, a value suitable for converters. Additionaly, the system exhibits high DC gain at low frequencies, which is beneficial for minimizing steady-state error. However, the step response analysis indicates that this gain is insufficient to meet the desired steady-state performance criteria. To achieve the required level of steady-state accuracy, additional compensation is necessary. A lag compensator is proposed to increase the DC gain.

Lag compensator for VMC

The lag compensator works by enhancing low-frequency gain without significantly affecting the phase margin or crossover frequency. To increase the DC gain problem, a pole is placed at the origin. But only adding a pole at origin has some problem like decrease to bandwidth. Low bandwidth causes to slow dynamic response. To eliminate the effect of pole at origin, a zero is needed. The general form of lag compensator is equal to $\mathrm{Glag} = \frac{s+Z_{lag}}{s}$. After several iterations, the optimal lag compensator was determined as $\mathrm{Glag} = \frac{s+10000}{s}$. The Bode plot of the open-loop transfer function with the lag compensator is shown in Figure 5.10.

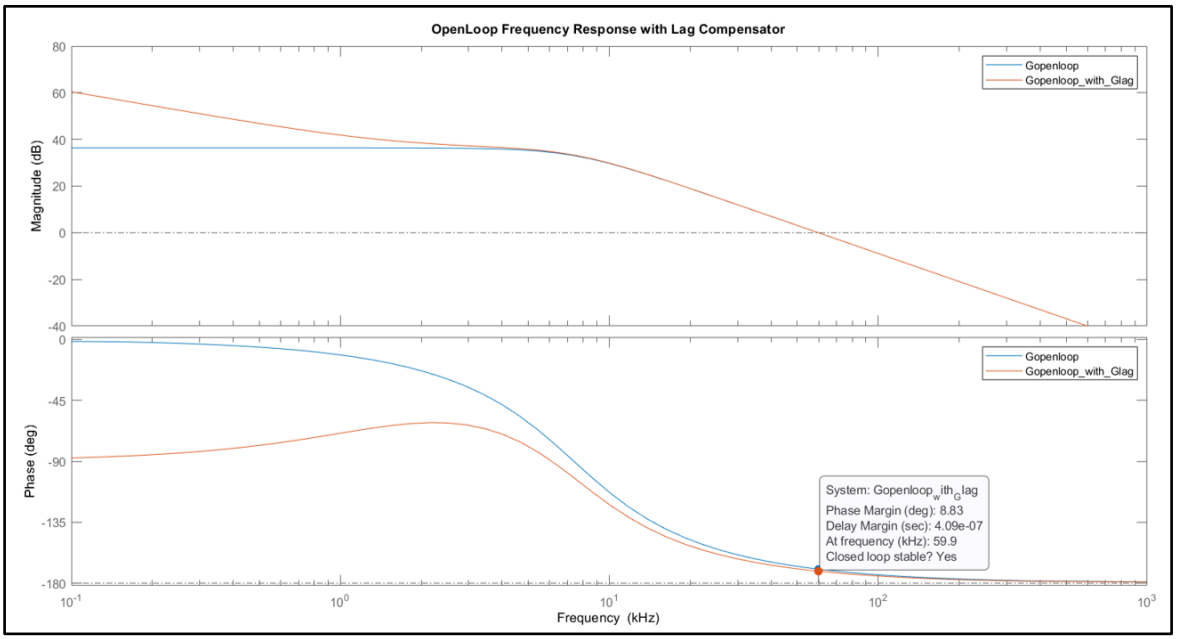

Figure 5.10. Bode plot of open loop transfer function with lag compensator

DC gain problem was eliminated. The lag compensator successfully eliminated the DC gain issue, ensuring accurate steady-state performance. The crossover frequency remained at approximately 1/8th of the switching frequency, confirming its suitability for converters. However, the system exhibits poor stability due to a low phase margin. As seen in Figure 5.10, the phase margin is 10.4°, falls too below the recommended range of 45°–90°, indicating the system's instability. To address this, a lead compensator will be designed to improve the phase margin, ensuring a stable and well-performing closed-loop system.

Lead compensator for VMC

Phase margin should be larger than 45° for a stable system and a lead compensator is used to provide the needed phase margin for stability. The general form of lead compensator is equal to $\mathrm{Glead} = \mathrm{k_{lead}} \frac{(s+Z_{lead})}{(s+P_{lead})}$. The formulas and design step given below are used for lead compensator design.

Necessary to find required phase margin:

$$\xi = \sqrt{\frac{\ln^2(M_p)}{\pi^2 + \ln^2(M_p)}} \tag{5.2}$$

Mp is the percent overshoot. For load transient response less than 10% of Vo, Mp is equal to 0.1.

$$\xi = \sqrt{\frac{\ln^2(0.1)}{\pi^2 + \ln^2(0.1)}} = 0.5912 \tag{5.3}$$

Required phase margin:

$$\phi_m = \tan^{-1}\frac{2\xi}{\sqrt{-2\xi^2 + \sqrt{4\xi^4 + 1}}} \tag{5.4}$$

$$\phi_m = \tan^{-1}\frac{2 * 0.5912}{\sqrt{-2 * 0.5912^2 + \sqrt{4 * 0.5912^4 + 1}}} = 58.6° \quad (5.5)$$

Maximum Phase Margin:

$$\phi_{max} = \phi_m - \phi_{m_{uncompansated}} + 10 = 58.6° - 8.83° + 10 = 59.76° \quad (5.6)$$

Necessary to find Gleadmax, klead, Zlead and Plead:

$$\beta = \frac{1 - \sin(\phi\,max)}{1 + \sin(\phi\,max)} = \frac{1 - \sin(59.76)}{1 + \sin(59.76)} = 0.073 \quad (5.7)$$

Maximum Gain at the lead:

$$Glead_{max} = 20\log\frac{1}{\sqrt{\beta}} = 20\log\frac{1}{\sqrt{0.073}} = 26.17\ dB \quad (5.8)$$

Before determining klead, Zlead and Plead, it is essential to identify the frequency at which the gain is maximized. This frequency is calculated using the transfer function of the system with the lag compensator applied. The Bode diagram of the open-loop transfer function with the lag compensator, expressed in radians, is presented again in Figure 5.11.

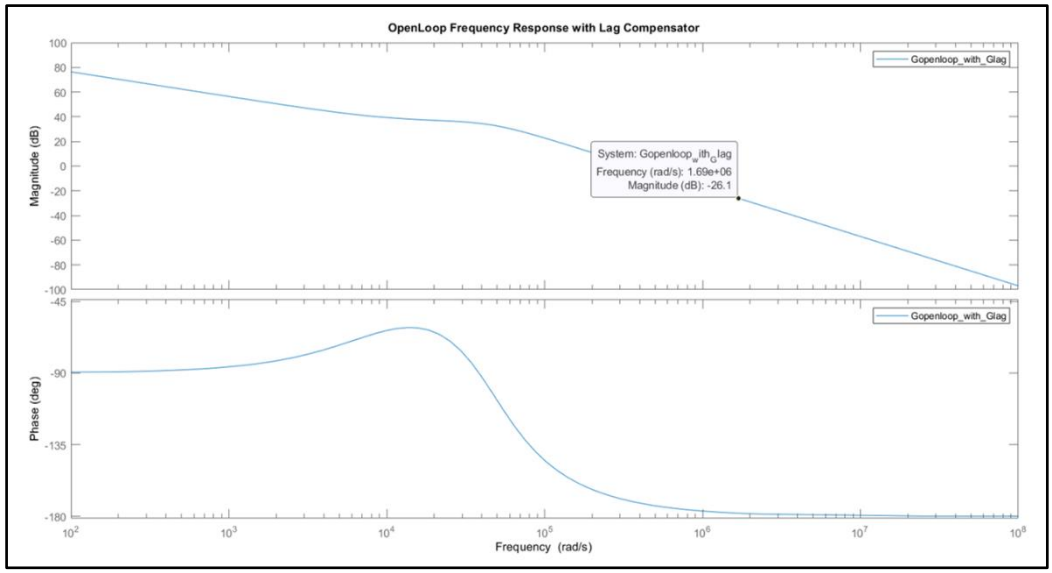

Figure 5.11. Bode plot of open loop transfer function with lag compensator (radians)

As seen in Figure 5.11, the frequency where gain is maximum ω_{max}= 1690000 rad/sec.
Constant of lead compensator:

$$k_{lead} = \frac{1}{\beta} = \frac{1}{0.073} = 13.70 \tag{5.9}$$

Zero of lead compensator:

$$Z_{lead} = \omega_{max}\sqrt{\beta} = 1690000 * \sqrt{0.073} = 456612.85 \tag{5.10}$$

Pole of lead compensator:

$$P_{lead} = \frac{Z_{lead}}{\beta} = \frac{456612.85}{0.073} = 6254970.54 \tag{5.11}$$

Every parameter in lead compensator was determined.

$$Glead = k_{lead}\frac{(s + Z_{lead})}{(s + P_{lead})} = 13.70\frac{(s + 456612.85)}{(s + 6254970.54)}$$

The Bode plot of the open-loop transfer function with the lag and lead compensator is shown in Figure 5.12.

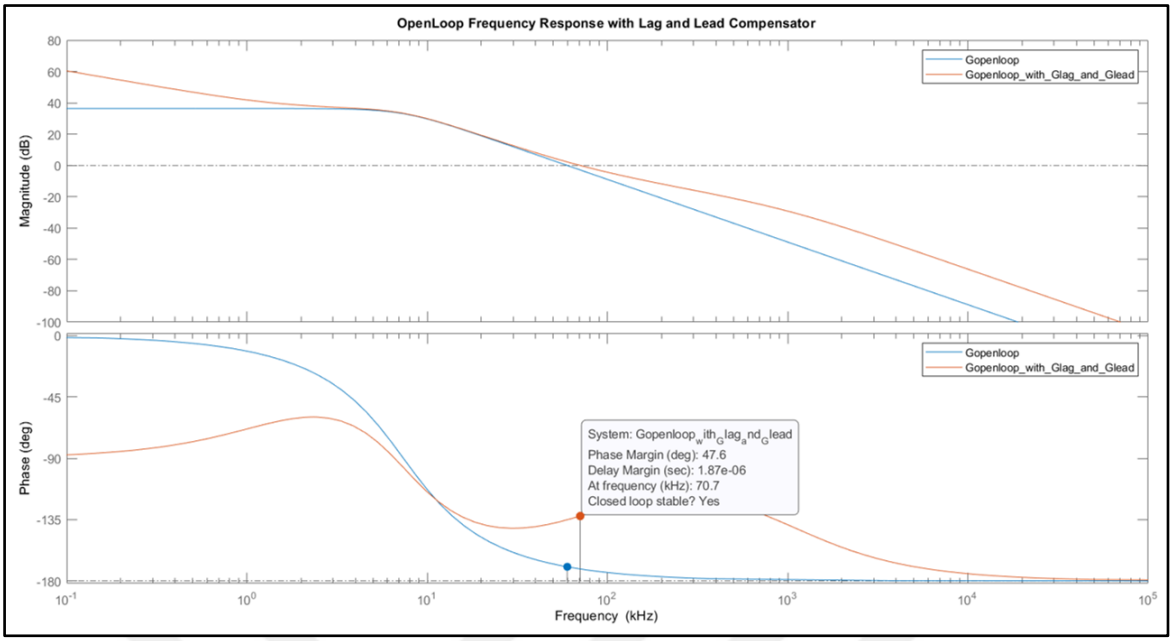

Figure 5.12. Bode plot of open loop transfer function with lag and lead compensator

The Bode plot of the open-loop transfer function with both the lag and lead compensators is shown in Figure 5.12. The compensated system achieves a phase margin of 47.6°, which falls within the recommended range for a stable system. Additionally, the crossover frequency is approximately 70 kHz, which is about 1/7th of the switching frequency, maintaining compatibility with the converter's operational requirements.

The final compensated system is shown in Figure 5.13, and its step response is illustrated in Figure 5.14. These results confirm that the designed compensators meet the performance and stability criteria for the PSFB converter.

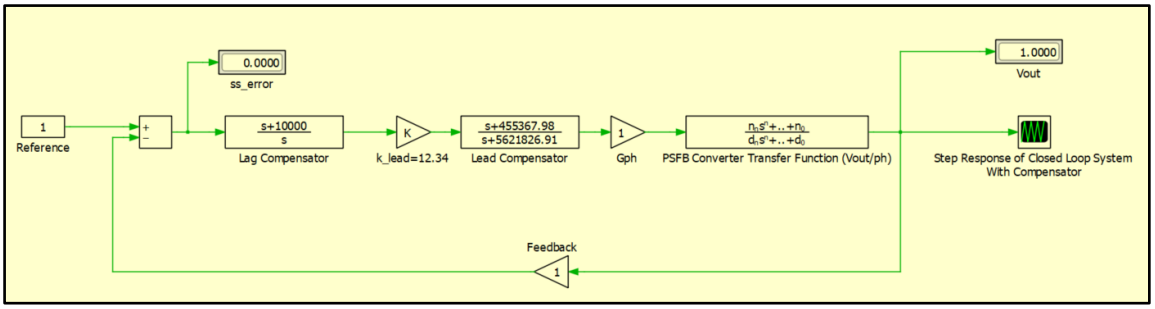

Figure 5.13. Lag and lead compensated system closed loop schema for step response

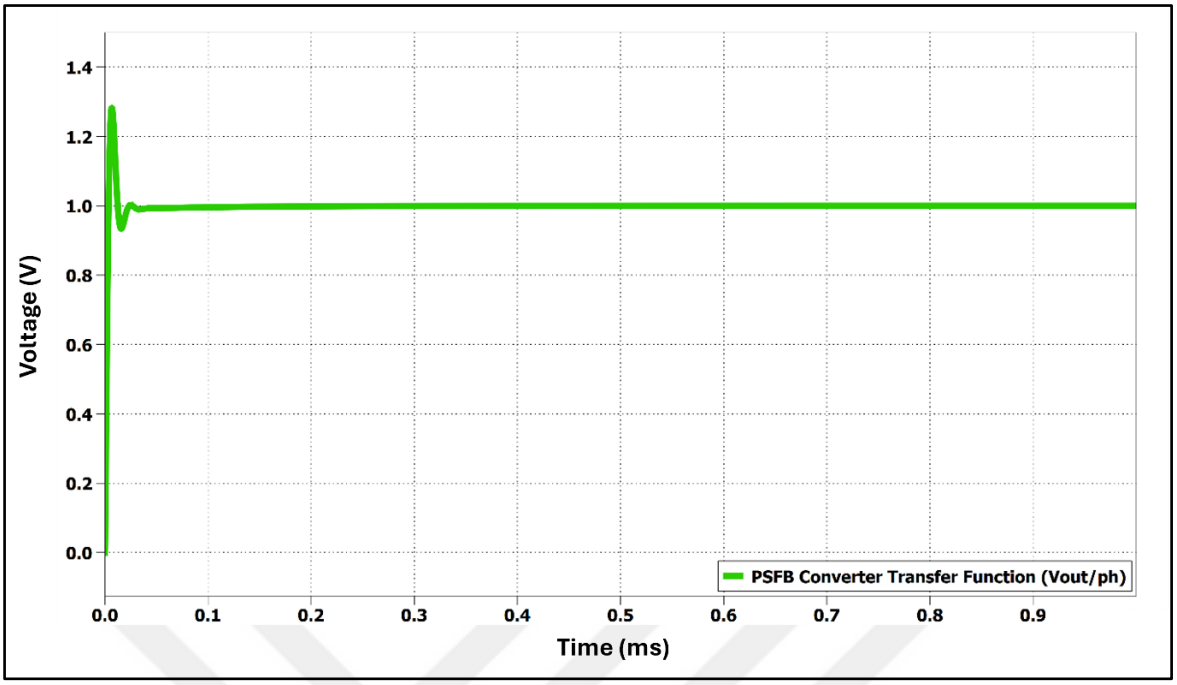

Figure 5.14. Step response of lag and lead compensated system

5.2. Current Mode Controller

In addition to VMC, in this study CMC has been improved. In VMC, the controller directly regulates the output voltage by comparing it to a reference voltage. The error signal is fed to a compensator, which adjusts the phase shift of the PWM to maintain the desired output voltage. The system essentially modulates the voltage without directly sensing the inductor current. In CMC, the controller not only regulates the output voltage but also senses the current flowing through the inductor or the power MOSFET. The current is used as a second control loop, effectively turning the system into a two-loop control structure: an inner current loop and an outer voltage loop. The inner loop modulates the inductor current, while the outer loop adjusts the voltage. The general multiloop system is shown in Figure 5.15.

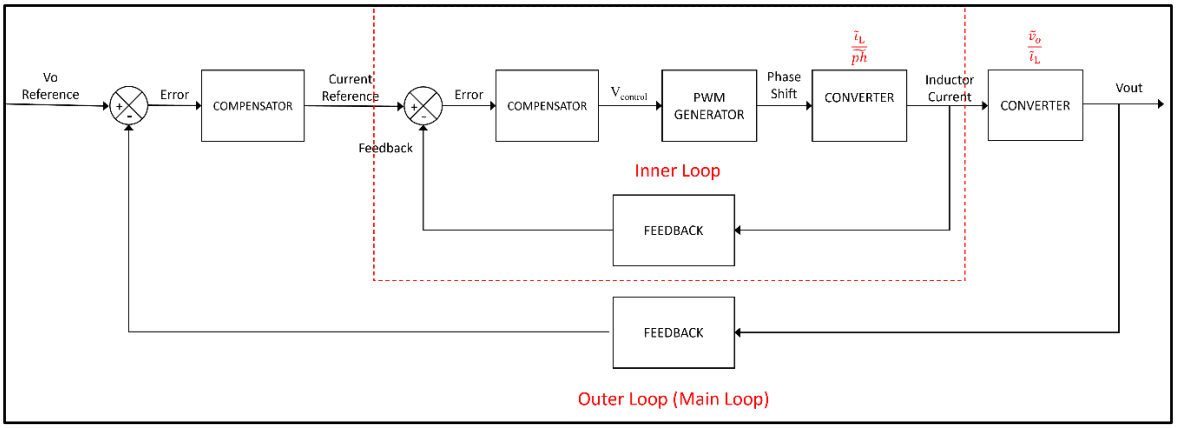

Figure 5.15. General multiloop control closed loop system diagram

CMC can be implemented in two primary forms; peak current mode control and average current mode control (ACMC).

Peak current mode control

In this method, the inductor current's peak value is sensed and used to regulate the system. While simpler to implement, peak current mode control can suffer from instability at higher duty cycles due to subharmonic oscillations, requiring additional compensation such as slope compensation.

Average current mode control

In this approach, the average value of the inductor current is sensed and controlled. This method provides better accuracy in current regulation and avoids the instability issues seen in peak current mode control, especially in applications with higher duty cycles. However, it is slightly more complex to implement due to the need for additional filtering and signal processing.

For this study, ACMC is employed due to its superior current regulation accuracy and stability under a wide range of operating conditions. ACMC ensures that the inductor current closely follows the desired reference while maintaining the robustness of the outer voltage loop. This combination makes ACMC particularly suitable for high-performance power converters like the PSFB.

5.2.1. Modelling of PSFB converter for CMC

As mentioned before, accurate modelling of converter is important for controller design. The converter model must capture the key dynamics of the converter. The transfer function of the inner loop is provided in “Eq 5.12”, while the transfer function of the outer loop is given in “Eq 5.13”.

$$\frac{\tilde{\imath}_{L_o}}{\widetilde{\mathrm{ph}}} = \frac{\mathrm{V_{in}}\frac{\mathrm{N_s}}{\mathrm{N_p}}\left(\mathrm{sC}+\frac{1}{\mathrm{R}}\right)}{\mathrm{s^2LC}+\mathrm{s}\left(\frac{\mathrm{L}}{\mathrm{R_o}}+2\left(\frac{\mathrm{N_s}}{\mathrm{N_p}}\right)^2\mathrm{f_{sw}L_KC}\right)+\frac{2\left(\frac{\mathrm{N_s}}{\mathrm{N_p}}\right)^2\mathrm{f_{sw}L_K}}{\mathrm{R_o}}+2} \tag{5.12}$$

$$\frac{\tilde{\mathrm{v}}_{\mathrm{o}}}{\tilde{\imath}_{L_o}} = \frac{2}{sC+\frac{1}{R}} \tag{5.13}$$

The behavior of the small-signal model was evaluated by comparing it with the circuit model through PLECS simulations. The circuit schematic is shown in Figure 5.16, while the comparison results for the inner loop and outer loop are presented in Figure 5.17 and Figure 5.18**,** respectively.

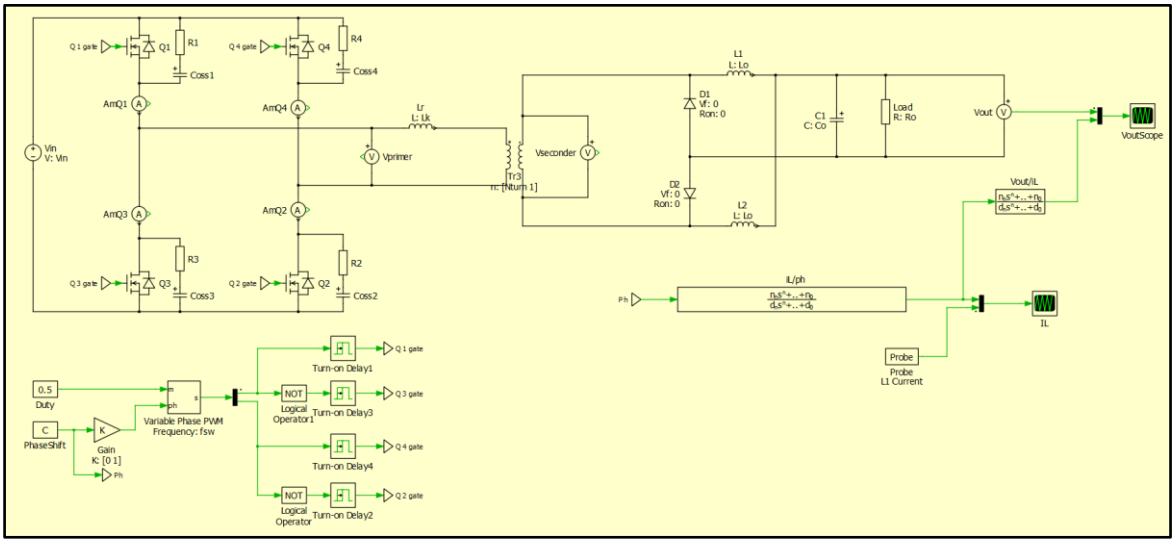

Figure 5.16. Circuit model for CMC

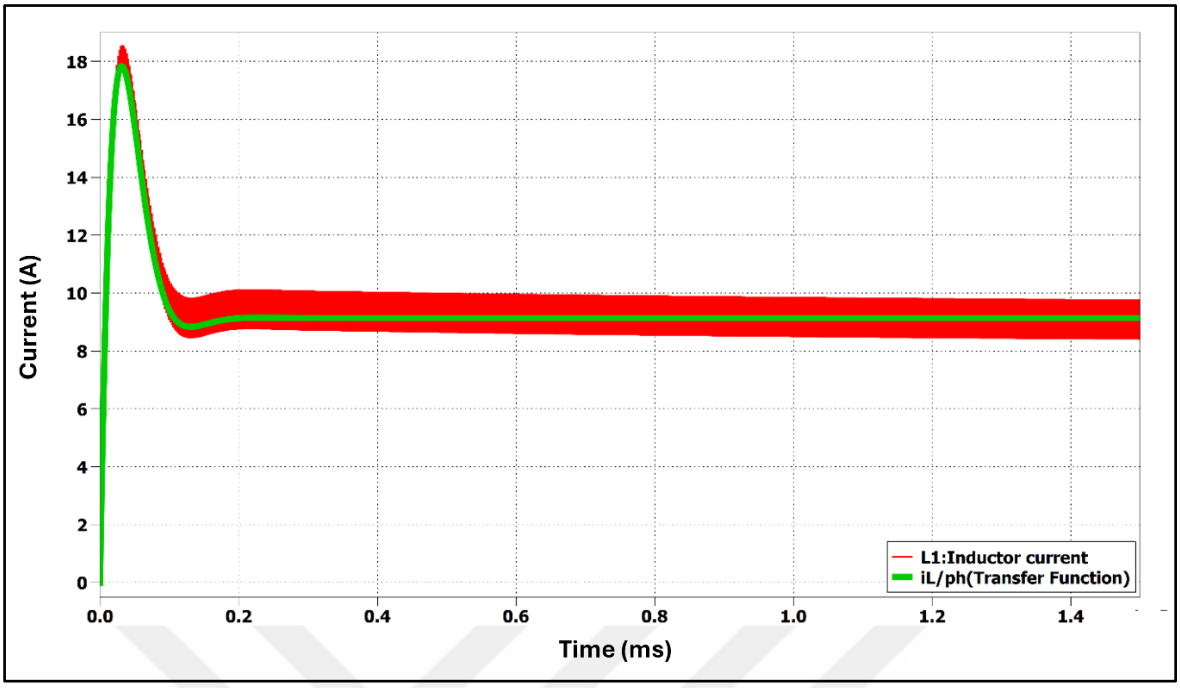

Figure 5.17. Comparison of the result of PSFB converter transfer function(iL/ph)

This figure compares the simulated and modeled responses of the inner loop, which regulates the inductor current based on the phase shift. The results confirm the accuracy of the small-signal model in capturing the key dynamics of the inner loop.

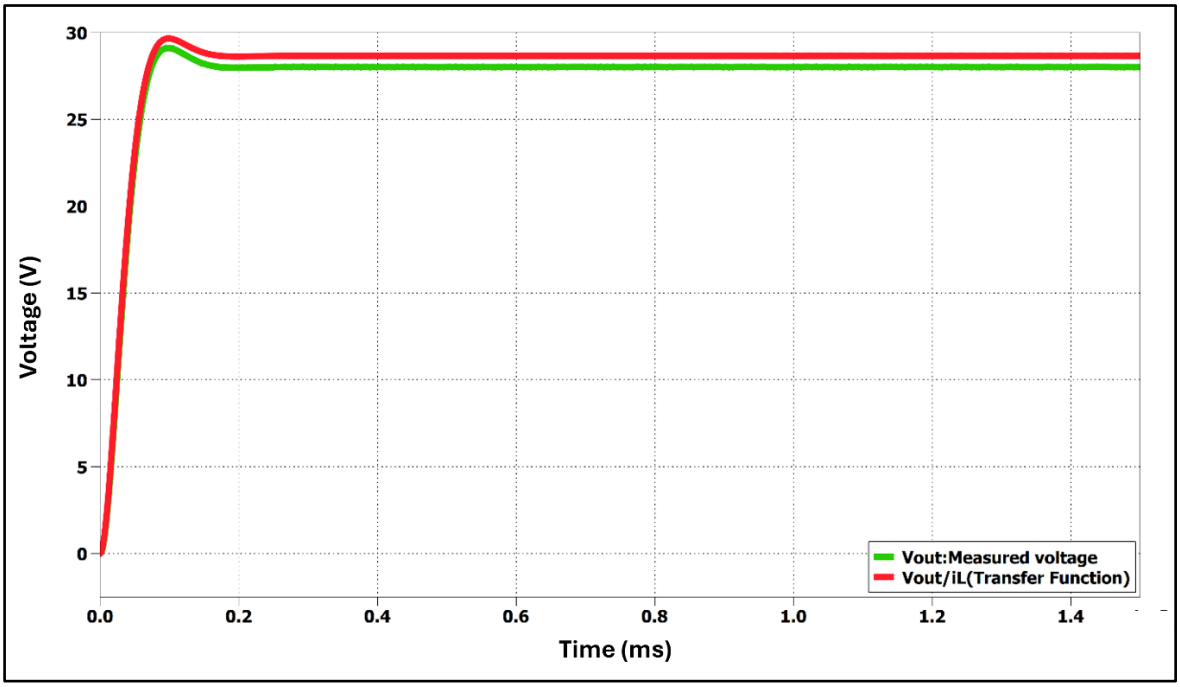

Figure 5.18. Comparison of the result of PSFB converter transfer function(Vout/iL)

This figure illustrates the agreement between the simulated and modeled responses of the outer loop, which governs the output voltage regulation. The close match validates the effectiveness of the outer-loop model.

These comparisons demonstrate that the small-signal model accurately represents the converter's behavior, making it a reliable foundation for designing robust controllers.

5.2.2. Compensator design for CMC

Before starting the compensator design, the last situation of closed loop system for ACMC is given in Figure 5.19.

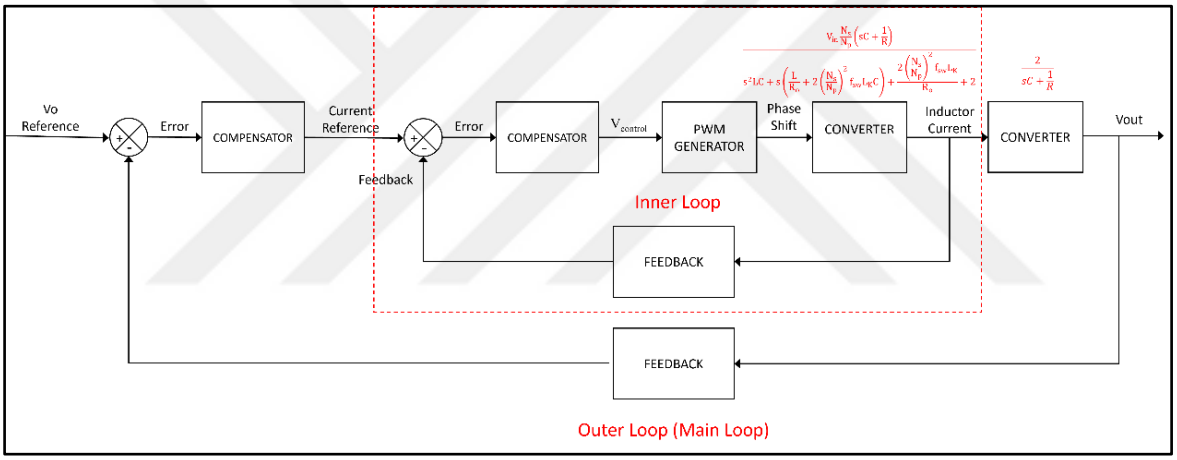

Figure 5.19. Closed-loop system for ACMC before compensator design

To assess system stability and dynamic performance, the step response of the closed-loop system was analyzed as in “Compensator design for ” section. Figure 5.20 illustrates the configuration used to simulate the step response of the system without compensation. The simulation results, presented in Figure 5.21. Step response without compensator, reveal the system's response to a step input.

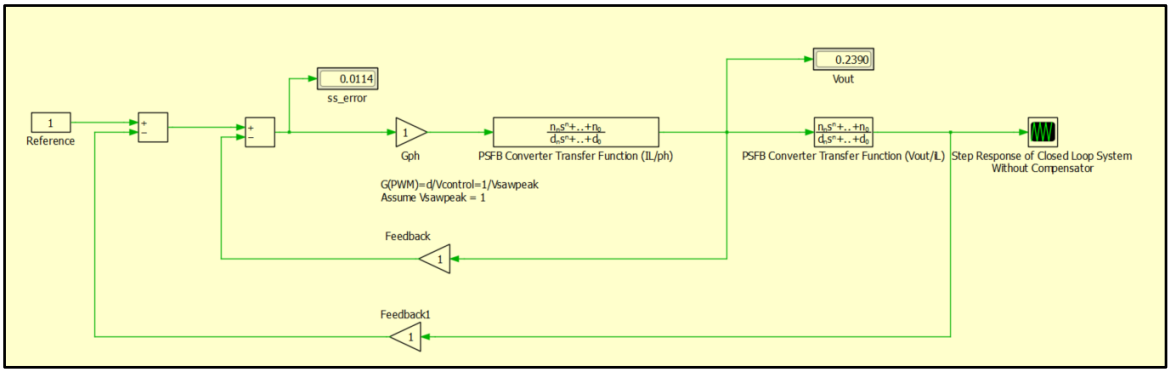

Figure 5.20. Closed-loop system for ACMC step response schema without compensator

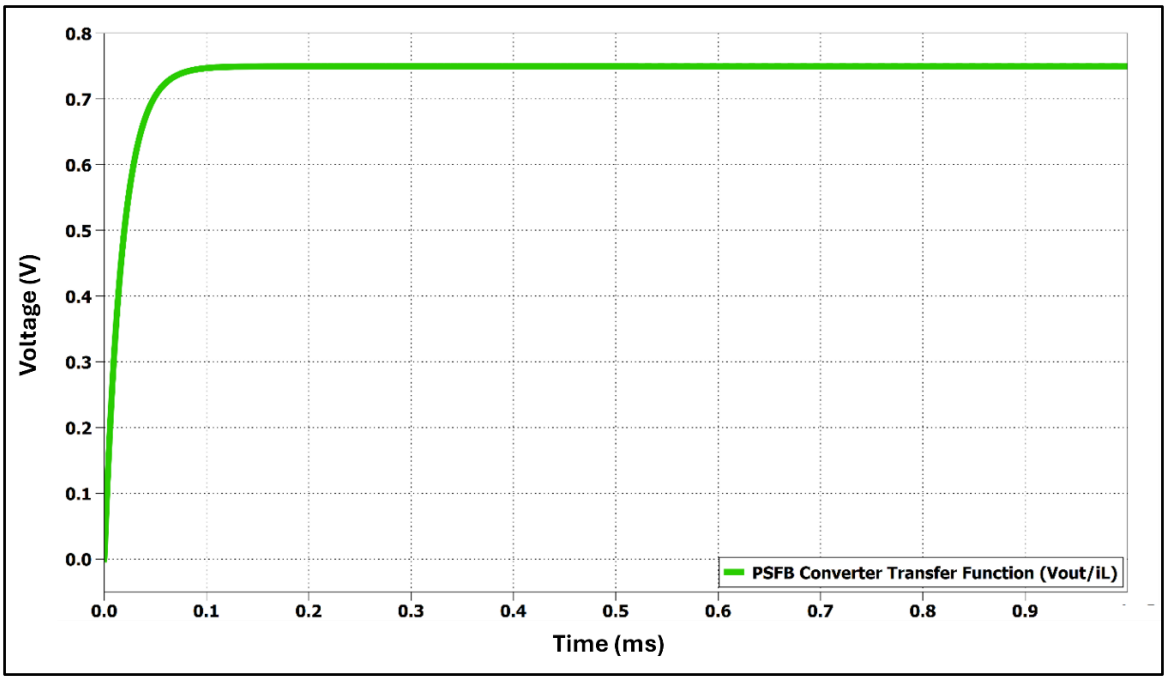

Figure 5.21. Step response without compensator

The simulation results indicate that the system is stable; however, a significant steady-state error persists. To address this issue, compensator design is necessary. Unlike VMC, CMC requires separate controller designs for both the inner and outer loops.

Inner loop controller design

The design of the inner loop controller is based on the small-signal model, with the assessment criteria outlined in the “Compensator design for ” section. To determine the characteristics of the compensator, the open-loop transfer function of the inner loop must

first be obtained. This requires breaking the closed-loop system after the feedback network. The broken closed-loop system for the inner loop is shown in Figure 5.22.

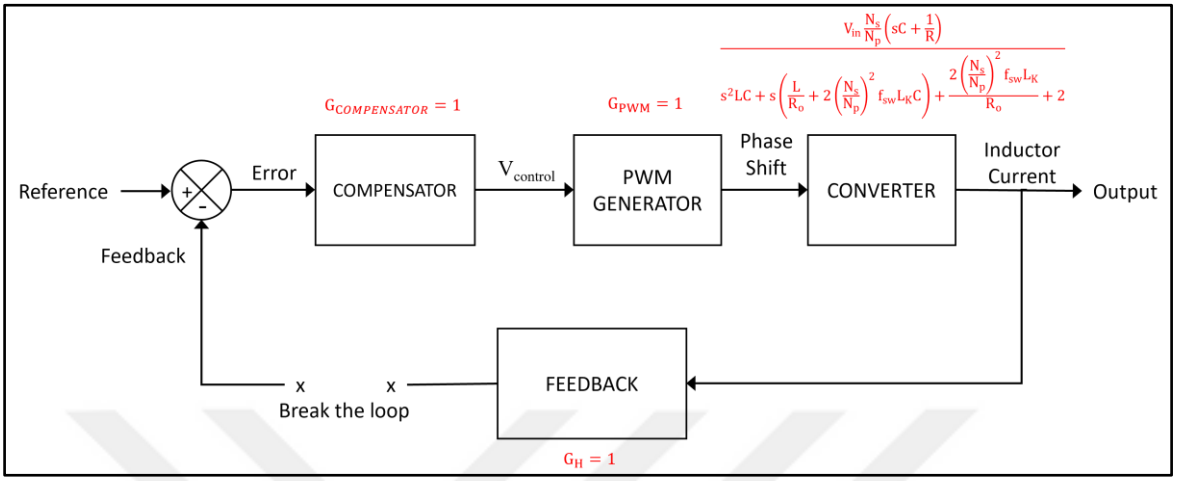

Figure 5.22. Broken closed-loop system of inner loop

Once the loop is broken, the open-loop transfer function corresponds to the inner-loop transfer function of the converter. The Bode plot of the open-loop transfer function, generated using MATLAB, is presented in Figure 5.23.

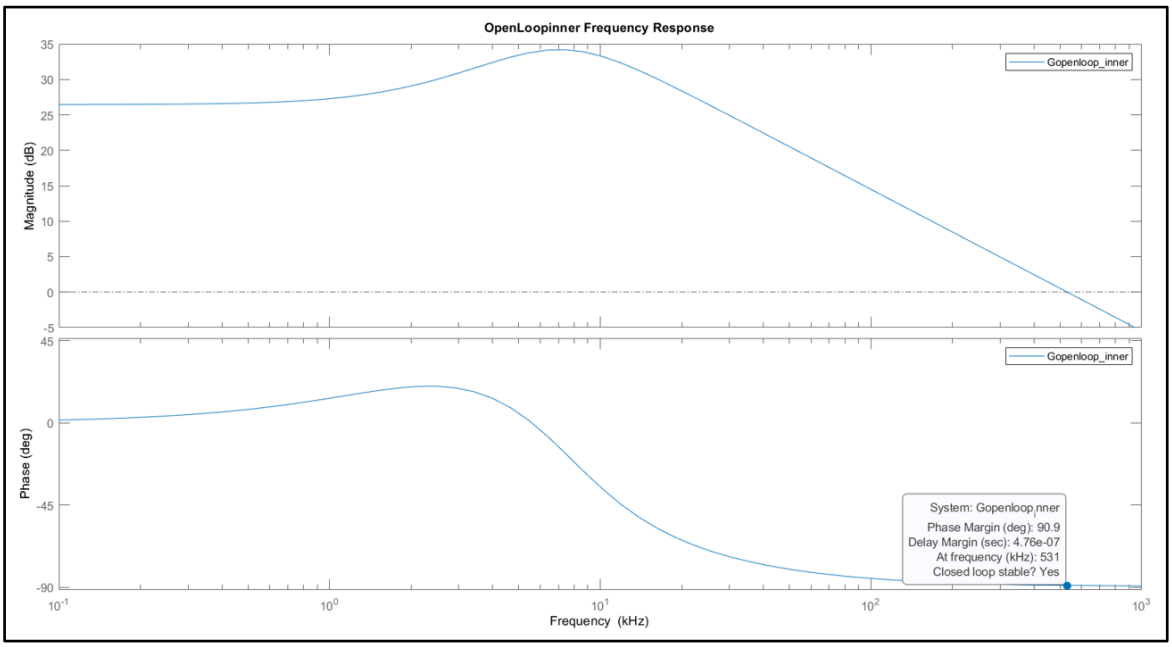

Figure 5.23. Bode plot of open loop inner transfer function

The analysis of the Bode plot reveals that the system is stable with a phase margin of 90°. However, the crossover frequency is excessively high at 531 kHz, which poses a risk of amplifying switching noise. To ensure noise immunity, the gain at the switching frequency must be minimized. As a general guideline, the crossover frequency should be approximately 1/15th of the switching frequency.

To reduce the crossover frequency to the desired level of approximately 30 kHz (1/15th of fsw), a proportional gain (kp) of 0.055 was introduced before the compensator block. The effect of this proportional gain is shown in Figure 5.24.

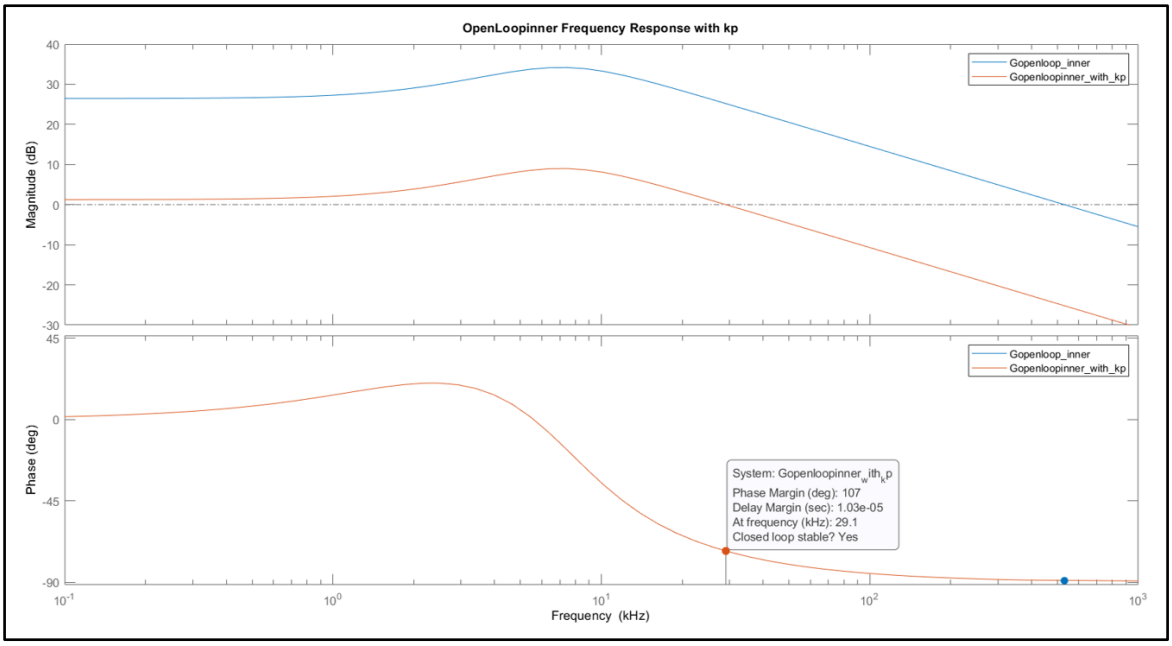

Figure 5.24. Bode plot of open loop inner transfer function with kp

While kp < 1 successfully addresses the high crossover frequency, it also reduces the DC gain, which adversely impacts steady-state performance. To restore the DC gain and improve steady-state accuracy, a lag compensator was introduced. After several design iterations, the optimal lag compensator was determined to be: $\mathrm{Glag} = \frac{s+150000}{s}$. The Bode plot of the open-loop transfer function with the lag compensator is shown in Figure 5.25.

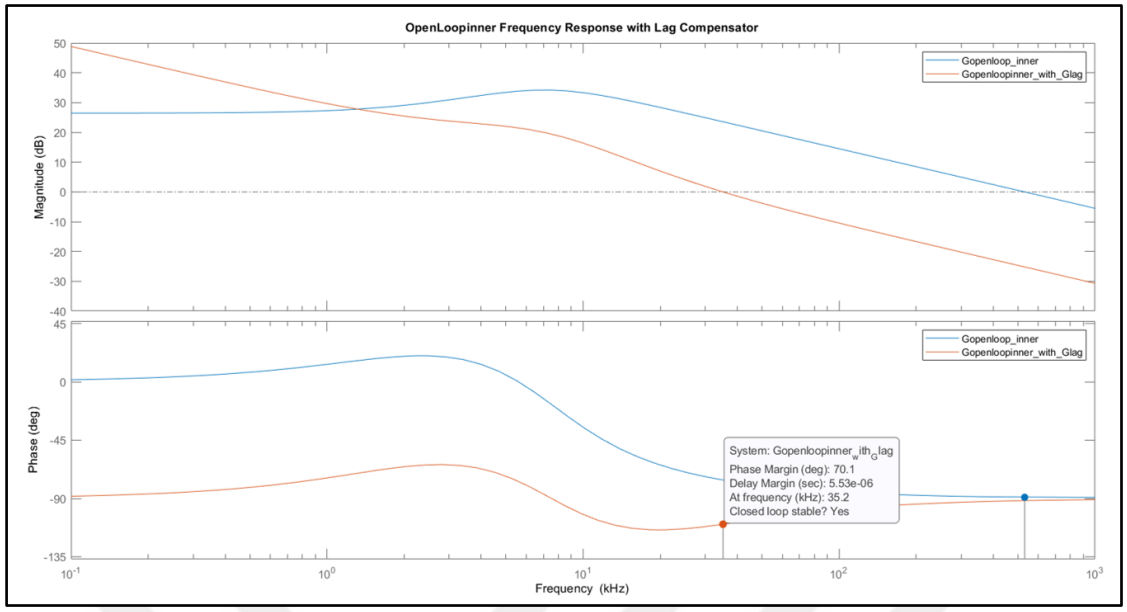

Figure 5.25. Bode plot of open loop inner transfer function with lag compensator

The combination of kp and the lag compensator effectively addresses both the high crossover frequency and low DC gain issues. With these adjustments, the inner loop achieves the desired performance, maintaining stability, reducing sensitivity to switching noise, and ensuring accurate steady-state operation.

Outer loop controller design

To design the compensator for the outer loop, the open-loop transfer function must first be obtained by breaking the closed-loop system after the feedback network. For this design, the inner loop is considered as unity (1) to simplify the analysis. The configuration of the broken closed-loop system for the outer loop is shown in Figure 5.26.

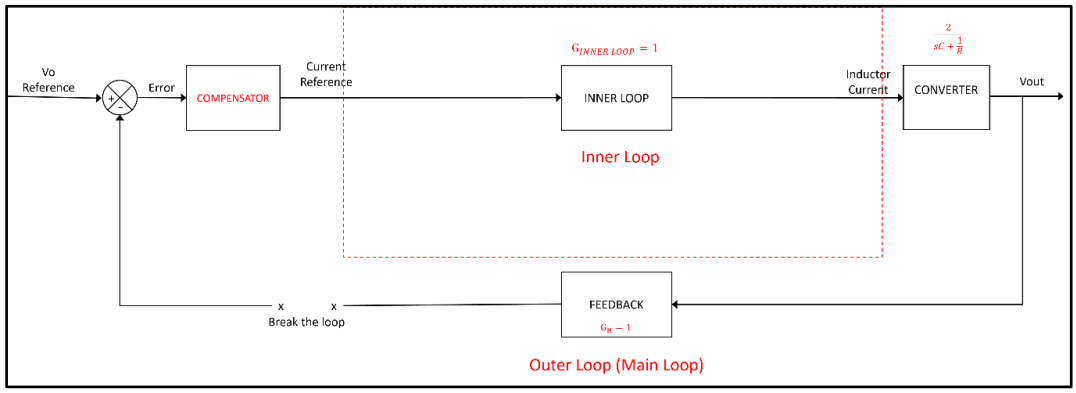

Figure 5.26. Broken closed-loop system of outer loop

Once the loop is broken, the open-loop transfer function corresponds to the outer-loop transfer function of the converter. The Bode plot of this open-loop transfer function, generated using MATLAB, is shown in Figure 5.27.

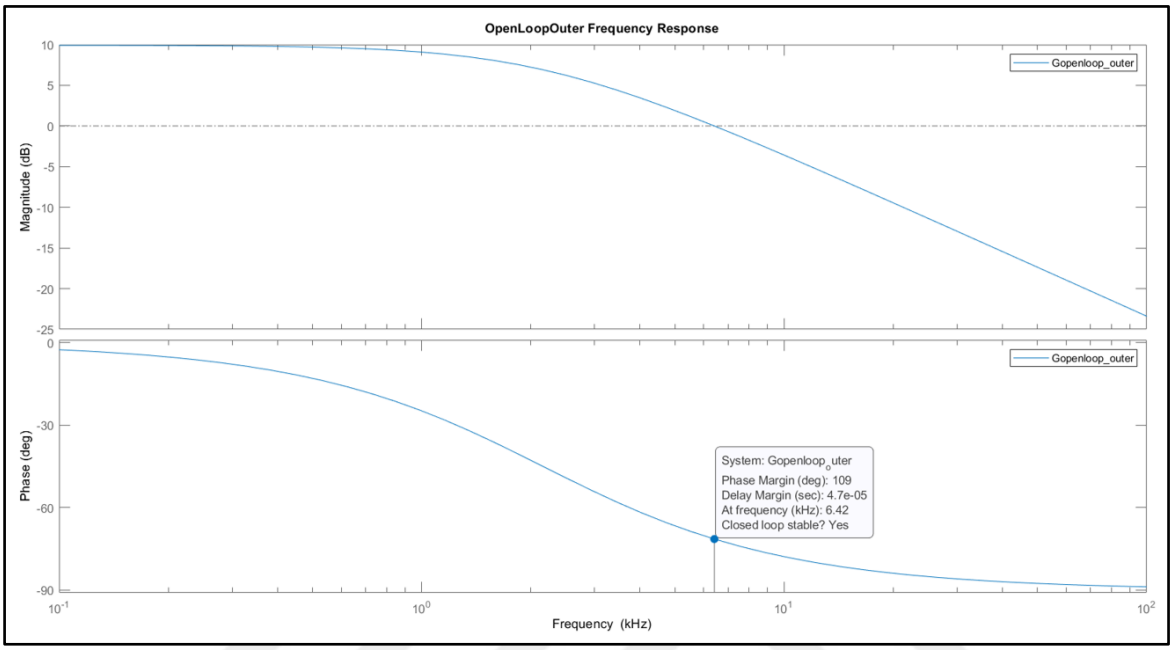

Figure 5.27. Bode plot of open loop outer transfer function

The analysis of the Bode plot reveals that the system is nearly stable but exhibits low DC gain, which could lead to poor steady-state performance. The crossover frequency, however, is appropriate for the outer loop. In ACMC, the crossover frequency of the inner loop is set to approximately 1/15th of the switching frequency. For the outer loop, the crossover frequency should typically be lower, around 1/60th of the switching frequency, to ensure proper separation of the two loops and to maintain stability. A lag compensator is sufficient to address the low DC gain of the outer loop. After several iterations lag compensator find as a $\mathrm{Glag} = \frac{s+20000}{s}$ for outer loop. The effect of the lag compensator on the outer-loop transfer function is shown in Figure 5.28. The lag compensator successfully increases the DC gain, ensuring accurate steady-state performance while maintaining the desired crossover frequency.

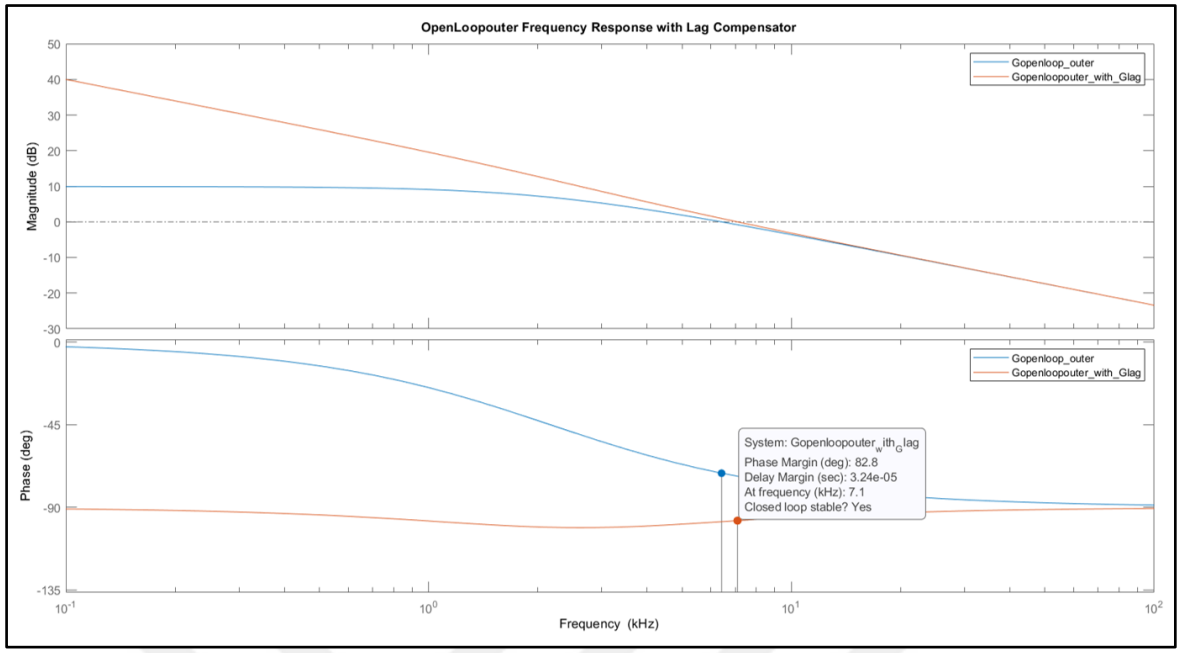

Figure 5.28. Bode plot of open loop outer transfer function with lag compensator

With the inclusion of this lag compensator, the outer loop meets all design requirements, achieving stability, adequate gain, and proper dynamic response. No additional compensators are necessary for the outer loop, confirming the effectiveness of the proposed design.

The effectiveness of the designed compensators was further validated by analyzing the step response of the fully compensated system. The final compensated system is depicted inFigure 5.29, and the corresponding step response is shown in Figure 5.30.

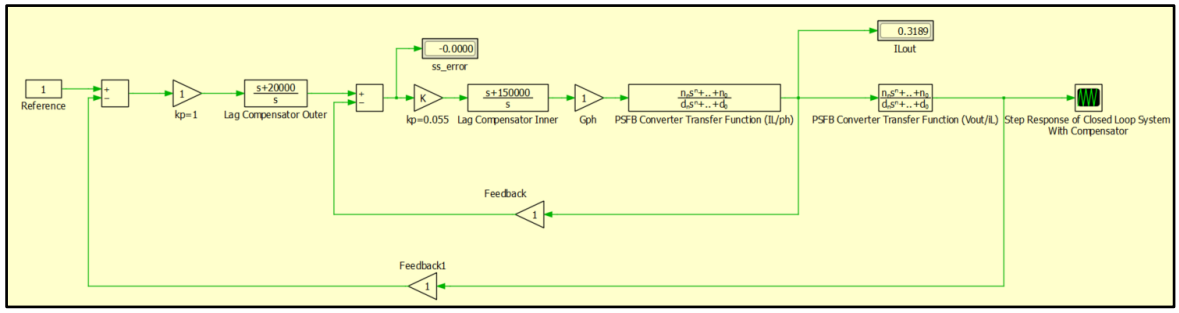

Figure 5.29. Lag compensated multiloop system closed loop schema for step response

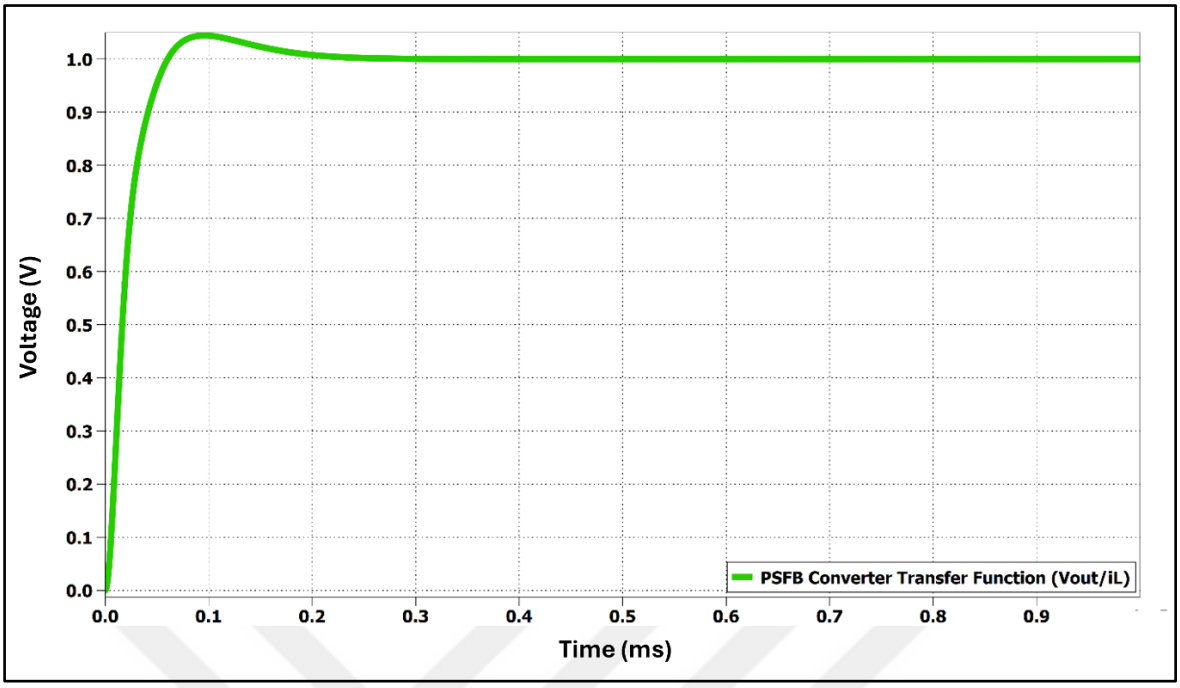

Figure 5.30. Step response of lag compensated multiloop system

The step response demonstrates the system's ability to maintain stability while achieving fast transient recovery and minimal overshoot. When subjected to a step change in the load, the output voltage settles quickly, indicating that the compensators are functioning effectively to regulate the system. The overshoot observed in the response is well within the acceptable range, ensuring that the converter operates without violating the specified limits.

5.3. Comparison of VMC and CMC

VMC and CMC are two widely used strategies for regulating power converters, each offering distinct methodologies and characteristics.

In VMC, the controller relies solely on output voltage feedback to regulate the converter. It employs a single control loop to adjust the phase shift of the PWM, ensuring that the output voltage matches the reference value. This simplicity makes VMC straightforward to implement; however, it does not account for inductor current, limiting its ability to handle current regulation and overcurrent protection effectively.

In contrast, CMC employs a dual-loop structure, incorporating both output voltage and inductor current feedback. The inner loop controls the inductor current, while the outer loop

regulates the output voltage. This architecture provides better dynamic response and enhanced current regulation capabilities, making it a more robust solution for applications requiring higher performance and safety.

In this study, both control strategies were implemented for the PSFB converter, and their performances were compared based on dynamic response, stability, and steady-state accuracy. The step response comparison of the two methods is shown in Figure 5.31 and the corresponding simulation results are presented in Figure 5.32.

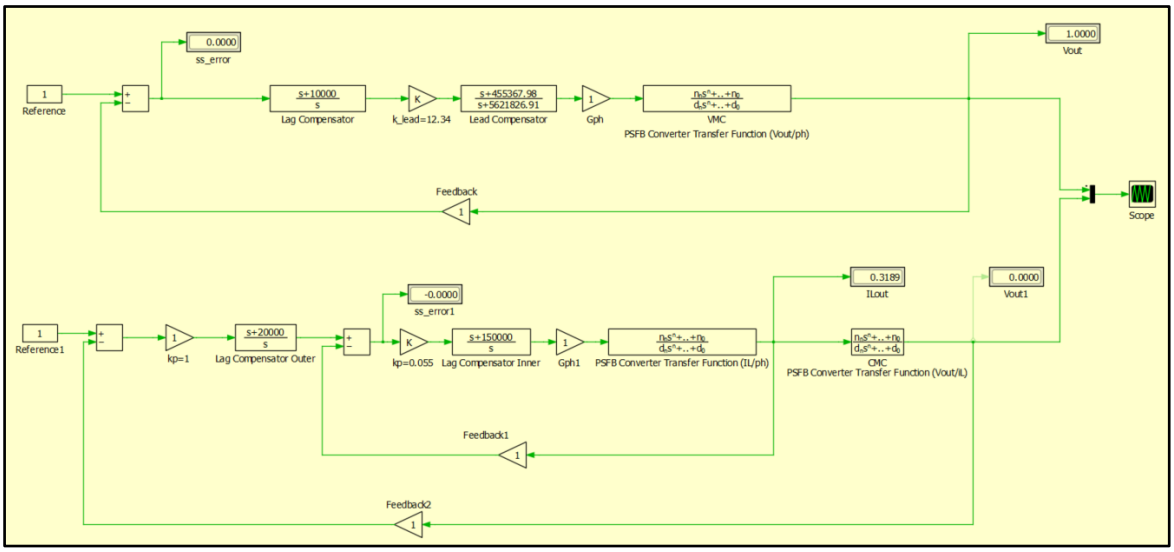

Figure 5.31. Step response comparison schema

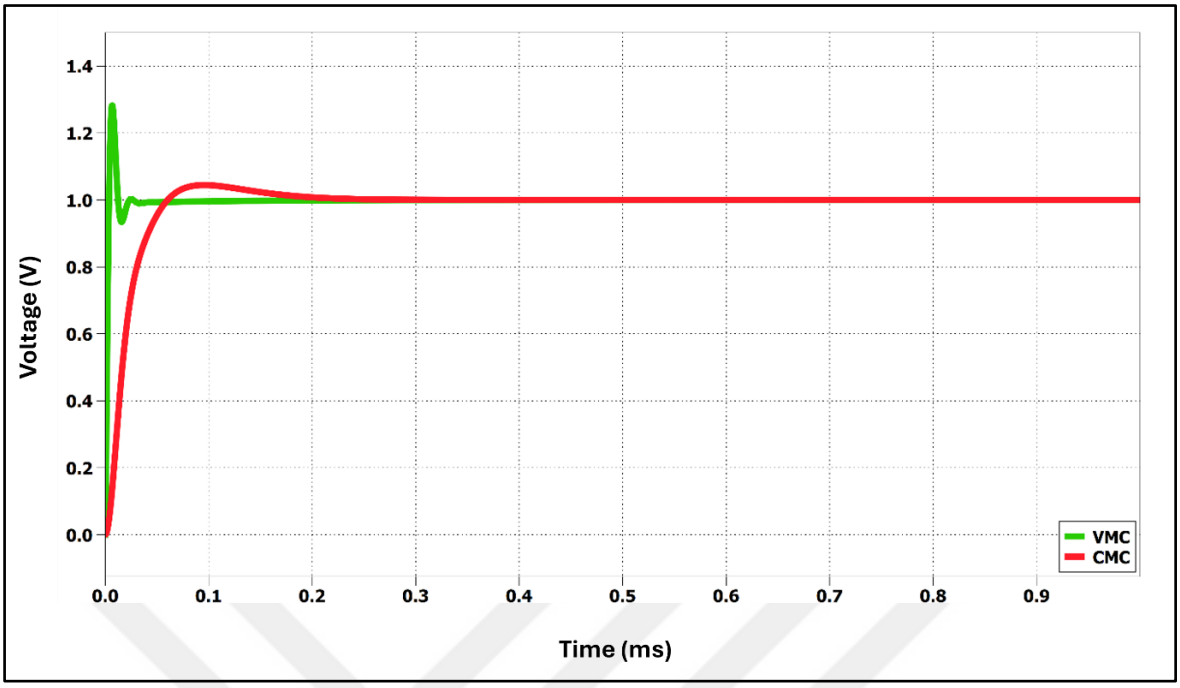

Figure 5.32. Step response comparison result

The step response simulations highlight the performance differences between the two control strategies. VMC exhibits faster transient recovery thanks to higher crossover frequency when subjected to a step change in load. The output voltage takes shorter to stabilize, but the overshoot is slightly larger. Both methods can achieve stable operation when properly compensated. There is no steady state error both control method.

Although VMC is simpler to implement due to its single control loop and reliance solely on voltage feedback, ACMC was selected for this study because of its distinct advantages. ACMC provides superior features, including inherent short-circuit current protection and effective current limiting, which are critical for ensuring system safety and reliability.
Additionally, the PSFB system was inherently stable under ACMC even before introducing the controller, which significantly simplified the compensator design. This allowed the controller design to be achieved using only a lag compensator, further highlighting the practicality and efficiency of this control strategy.

In summary, while both control strategies are suitable for regulating the PSFB converter, ACMC offers a more robust and reliable solution, making it the preferred choice for this study.

6. SIMULATION RESULTS

Simulation results are presented to validate the performance of the designed PSFB converter. The simulation of the ACMC controlled PSFB converter was conducted using PLECS to validate the theoretical analysis and design considerations discussed in the previous sections. The simulation environment allows for detailed observation of the converter's dynamic behavior under various operating conditions, including steady-state and transient responses. The key parameters used in the simulations align with the converter's specifications: an input voltage range of 200-400V, a switching frequency of 500kHz, and an output power of 500W with a regulated output voltage of 28V.

6.1. Steady-State Operation

The steady-state performance of the PSFB converter was evaluated to ensure that it meets the specified design requirements. The circuit schematic of the designed PSFB converter, including the ACMC strategy, is shown in Figure 6.1. The simulation results confirm that the converter operates stably across the entire input voltage range of 200–400V, consistently maintaining an output voltage of 28V, as illustrated in Figure 6.2.

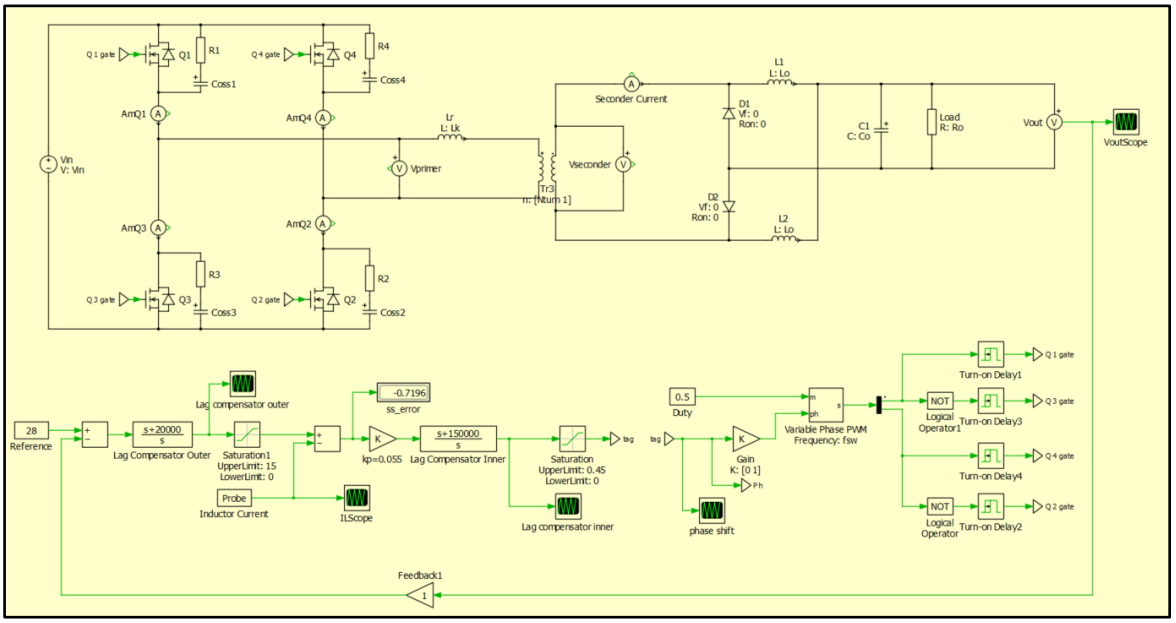

Figure 6.1. Designed PSFB converter with ACMC

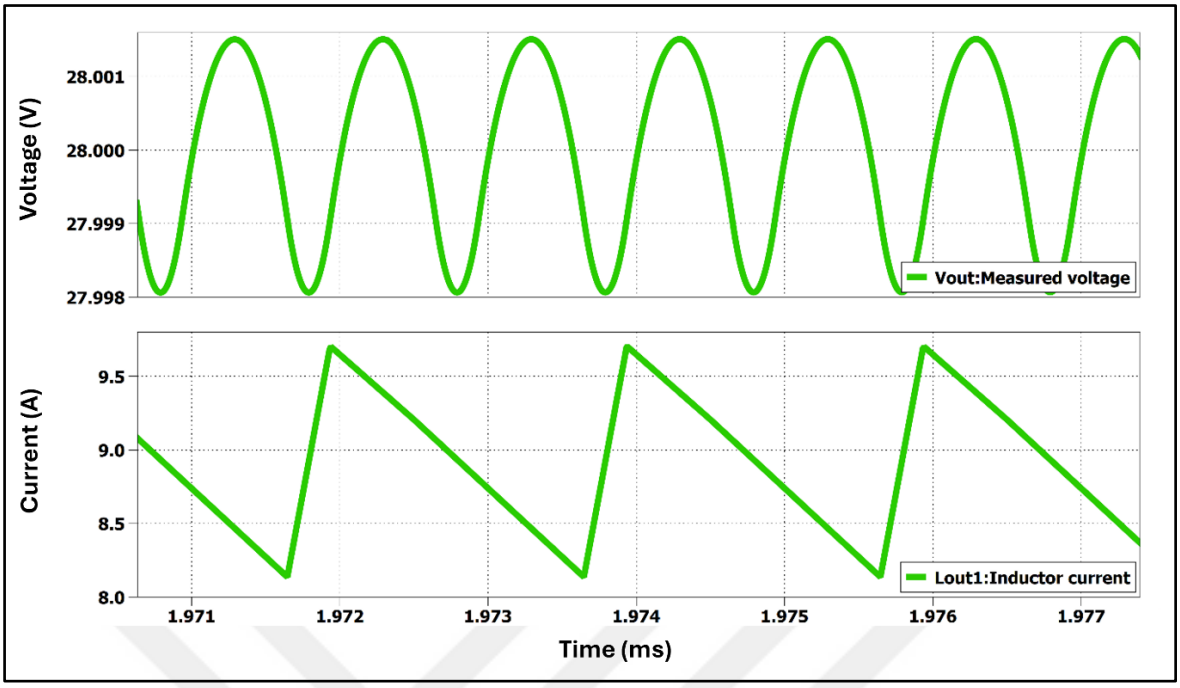

Figure 6.2. Output voltage and output ınductor current

The output voltage remains within the desired regulation limits, and the output inductor current exhibits a smooth and stable waveform, validating the effectiveness of the converter's design. The inductor current ripple is well within the specified range of 20%, ensuring the proper operation of the output filter and reducing stress on the load.

This steady-state analysis highlights the accuracy of the theoretical design and confirms that the converter performs as expected under normal operating conditions, providing a solid foundation for evaluating its dynamic performance.

6.2. Response to Load Variations

To evaluate the dynamic response of the PSFB converter, simulations were conducted to observe its behavior during sudden load variations. A load step was introduced in the simulation, starting from full load (100%) and then suddenly reducing to a light load (15%) before returning to full load. The circuit configuration used for this test is shown in Figure 6.3, while the output voltage response is presented in Figure 6.4.

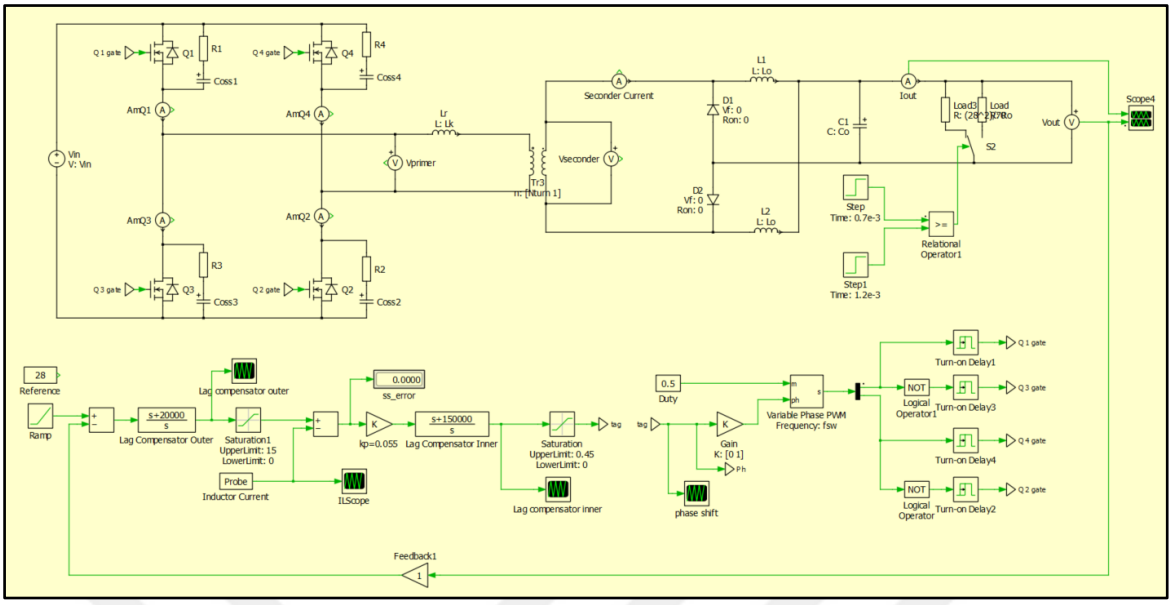

Figure 6.3. Circuit schema for load transient

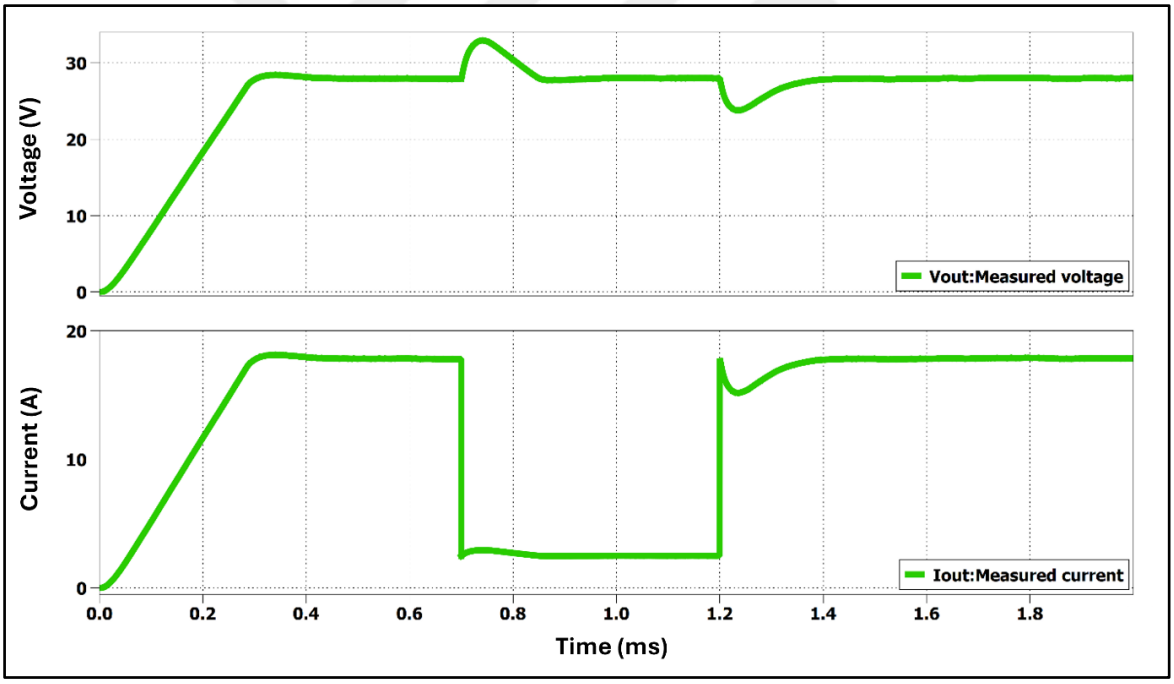

Figure 6.4. Output voltage response during load transient

The simulation results demonstrate that the converter responds effectively to abrupt changes in load. When the load is reduced, the output voltage experiences a minor transient but quickly stabilizes within the nominal range of 28V. Similarly, when the load returns to full capacity, the voltage transient is minimal, and the system rapidly regains steady-state operation.

These results highlight the robustness of the control strategy, ensuring reliable voltage regulation even under challenging dynamic conditions. The small voltage overshoot observed during load changes is well within acceptable limits, further validating the design's ability to handle load transients efficiently.

6.3. Input Voltage Variations

The converter's performance was also evaluated under varying input voltage conditions to confirm its ability to maintain output voltage regulation despite wide fluctuations in the input supply. During the simulation, the input voltage was varied linearly from 200V to 400V and then returned to 200V. The circuit configuration used for this test is illustrated in Figure 6.5, and the corresponding simulation results are shown in Figure 6.6.

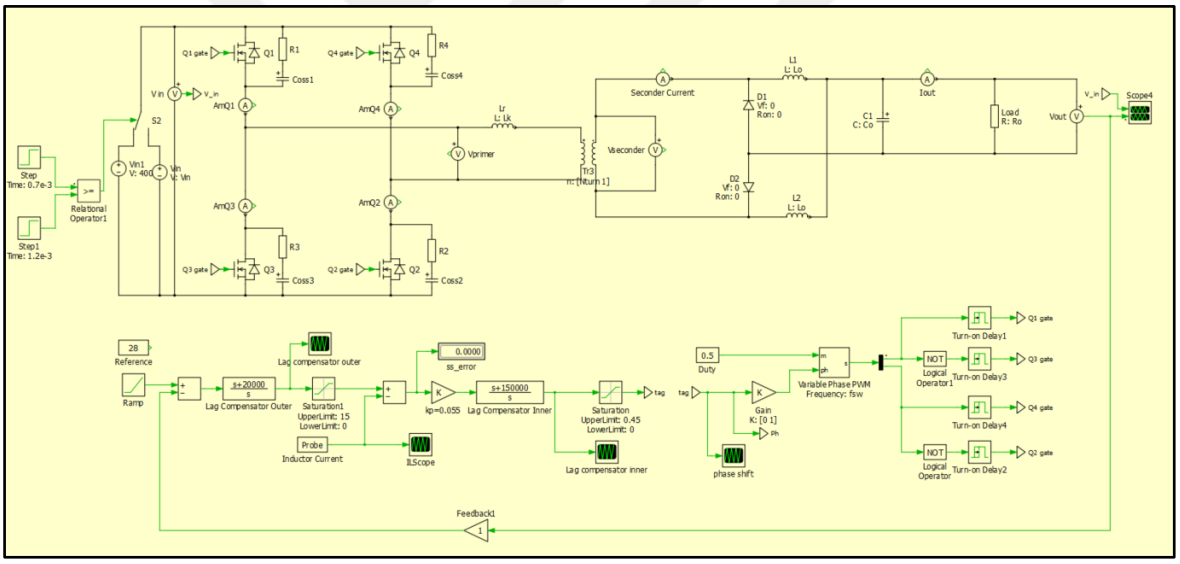

Figure 6.5. Circuit schema for load transient for input voltage transient

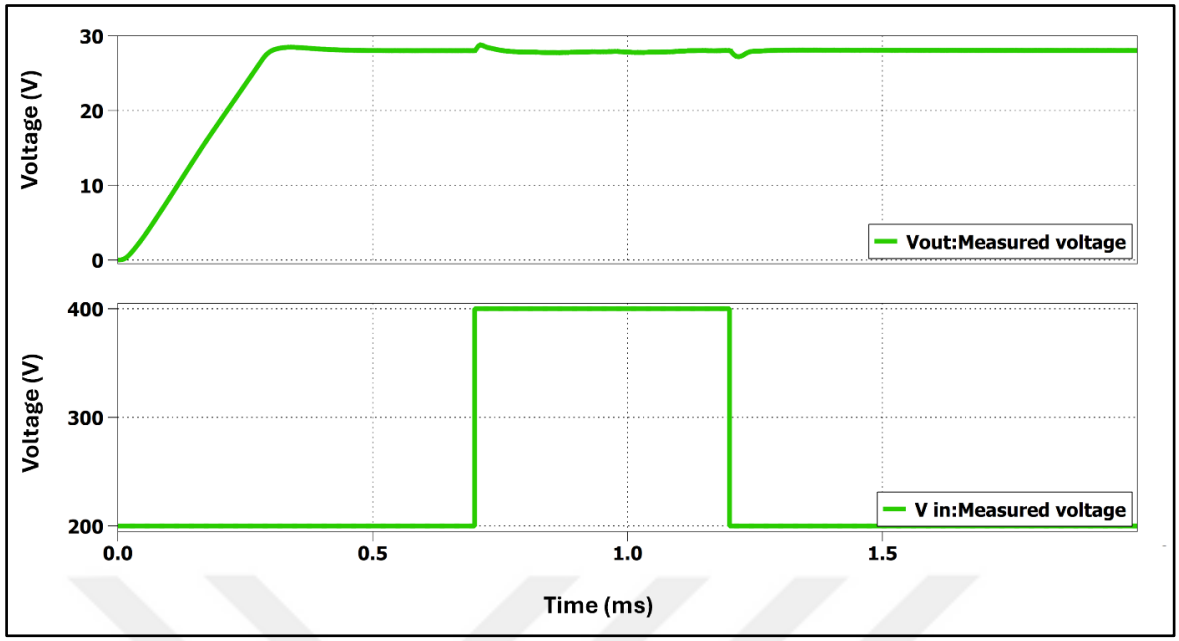

Figure 6.6. Output voltage response during input voltage transient

The results reveal that the output voltage remains well-regulated at 28V throughout the input voltage changes. The PSFB converter's control strategy effectively compensates for input voltage variations, ensuring that the output voltage stays within the specified range.

This capability is crucial in applications where input voltage may fluctuate due to supply instability or environmental factors. The simulation confirms the effectiveness of the converter design in handling such challenges, providing stable and reliable output performance.

6.4. ZVS Operation

The implementation of ZVS is a critical aspect of the PSFB converter design, enabling it to achieve high efficiency by minimizing switching losses. Simulations were conducted to verify ZVS operation under various load conditions. The results confirm that the converter achieves ZVS at a load of 250W, as illustrated in Figure 6.7.

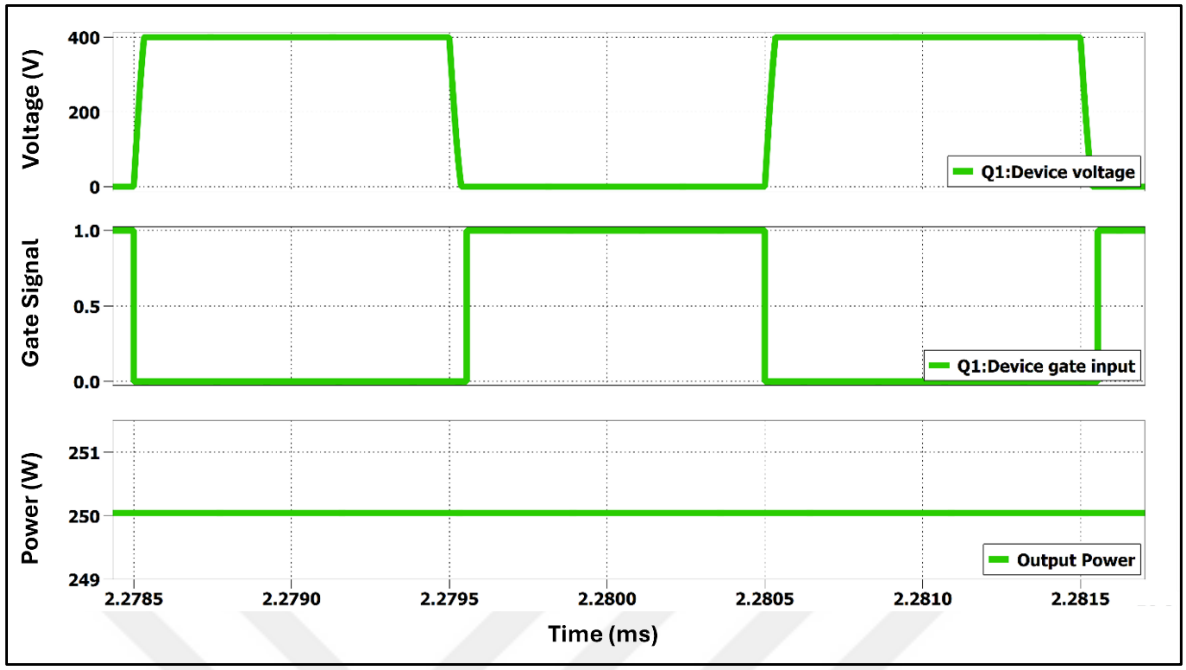

Figure 6.7. ZVS operation

The VDS of the MOSFETs drops to zero before the VGS signal turns them on, ensuring lossless switching during the turn-on transition. This behavior significantly reduces switching losses, leading to improved overall efficiency and reduced thermal stress on the power switches.

ZVS operation was observed across a wide load range, confirming the robustness of the design and its ability to maintain high efficiency in different operating conditions. These results align with the theoretical analysis and demonstrate the successful implementation of ZVS in the PSFB converter.

7. CONCLUSION AND RECOMMENDATIONS

This thesis focuses on the design and control of a GaN based PSFB converter for military applications. First of all, the design requirement of the system was determined to meet MIL-STD-1760 and MIL-STD-704 standards. The power interface was selected by evaluating MIL-STD-1760. Depending on the selected interface, the input voltage range, including transients, was set according to MIL-STD-704. The converter operates within a 200-400V input range, delivers 500W at 28V output, and operates at a high switching frequency of 500kHz. The high switching frequency was selected to achieve high power density.

Hard-switching and soft-switching topologies were evaluated. Since a high switching frequency is used, a soft-switching topology was chosen to reduce switching losses. The PSFB converter is one of the most popular soft-switching topologies and supports ZVS. This choice is also supported by using GaN MOSFETs. With GaN MOSFETs, the converter can operate at high frequencies and allow for a more compact design.

Each phase of the switching process of PSFB converter was analyzed to understand the roles of the switches, transformer, and other components. This detailed analysis guided the design choices for the power stage.

Key components like the transformer, GaN MOSFETs, diodes, inductors, and capacitors were carefully selected based on calculations. The transformer was designed with optimized leakage and magnetizing inductances to support ZVS. GaN MOSFETs were chosen especically according to low RDSon resistance because of soft switching contribute to eliminate switching loss. Low forward voltage diodes were used to minimize conduction loss. The output filter was designed to reduce voltage ripple. Output capacitor especially contribute to determine the output voltage overshoot. After selecting the key components, the design was verified through LTspice and PLECS simulations.

Controller design is the essential part of converter development. In this work, both VMC and CMC were designed for the PSFB converter. The transfer function of the converter was used as the basis for the controller design. Before starting the compensator design, the converter’s transfer function was compared with the circuit model using PLECS. The

controller design process was explained step by step. System stability was evaluated using Bode plots generated in MATLAB. During the design process, it was observed that the system was unstable without a compensator when using VMC. To stabilize the system, both lag and lead compensators were used in the VMC design. In contrast, the system was inherently stable without a compensator when using ACMC. Using only lag compensator meets system stability criterias in CMC. Both methods ensured system stability, however ACMC was selected for its simplicity and the added advantage of providing current protection.

The ACMC design was tested through simulations using PLECS software. LTspice simulations were used to verify the performance of individual components, while PLECS focused on analyzing the overall system behavior. The simulations confirmed that the converter met the design requirements, including stable output voltage, low ripple, and reliable operation under load and input voltage variations. Additionally, the converter achieved ZVS operation at loads of 250W and above.

Consequently, this thesis presents a detailed analysis, calculations, control methods, simulation models, and results for the PSFB converter. It demonstrates that GaN technology, combined with the PSFB topology, offers an effective solution for achieving high power density. Future work could focus on developing and testing a hardware prototype or exploring new control methods that consider low-load conditions. This study provides a foundation for converter designs.

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Gazili olmak ayrıcalıktır