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High-efficiency design of a grid-connected PV inverter based on interleaved flyback converter topology

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Abstract: The importance of efficiency in photovoltaic (PV) inverter applications makes the topology selection as the critical first step. Due to the low efficiency concern, flyback converter is not the preferred topology in kilowatt range in spite of its galvanic isolation, low cost, and small size advantages. Therefore, the objective of this research is to change the perception in favor of flyback converter by designing a flyback-topology-based PV inverter at 2.5 kW with high efficiency. The enhancement in efficiency is achieved mainly by using silicon carbide switching devices, designing ultrahigh-efficiency flyback transformers with extremely low leakage inductance and by implementing a prototype with the lowest parasitic components. As a result, the efficiency of the experimental inverter is measured as 95.82%. Moreover, the low cost and small size objectives are also maintained with very good grid side performance. Consequently, the experimental results demonstrated that the flyback-converter-topology-based inverters can be successfully implemented at high power with high efficiency and with high commercial value.

Key words: Flyback converter, interleaving, photovoltaic inverter, silicon carbide

1. Introduction

Depletion of fossil fuels and the growing environmental concerns due to the massive use of unclean fuels have increased interest in renewable energy sources. The solar energy technology has rapidly gained popularity due to its unlimited availability, which has reached a cumulative installed capacity of 303 GW by the end of 2016 [1]. This growth has been a great motivation to a significant number of research in power electronics field, including topology development and finding innovative solutions to obtain the best performance and the highest efficiency at the lowest cost.

The PV inverter proposed in [2] consists of two stages, a full-bridge inverter followed by a cycloconverter. The implemented system has 92.1% efficiency for 3 kW output. In [3], a series-resonant half-bridge converter is used in the DC-DC conversion stage of a 250 W PV inverter and it achieves 87% efficiency. In [4], a 300-W push-pull converter is utilized in the first stage of the inverter system. In [5], a ZVS resonant two-inductor boost converter topology is utilized as the DC-DC converter stage with 90% maximum efficiency. In [6], a current-fed two-inductor boost converter topology is used with a line frequency unfolder. The three-stage 100-W prototype achieves 92% efficiency. In [7], a PV inverter system with a soft-switching current-fed half-bridge DC-DC converter topology is proposed. It utilizes ZCS/ZVS and reports 91.2% maximum efficiency for a 200-W prototype. A hybrid series resonant and PWM boost converter topology is proposed in [8]. It can transfer

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power directly to the load and has the maximum efficiency of 98.32% for 300 W output. In [9], a 220-W single-stage CCM zeta microinverter reaches 93% efficiency.

The flyback-converter-topology-based inverters are attractive due to their simple structure and the low-cost advantages, but they are the choice of designers only at low power typically less than several hundred watts. Most of the commercial microinverters and AC power modules are therefore based on the flyback topology. It is the low efficiency concern that puts an upper limit on the power rating of the flyback-based converters. However, research has continued to see the merits of flyback topology and to explore the possibility of reaching high power without compromising the efficiency for flyback-based applications. A 100-W inverter based on cascaded flyback and buck-boost converter with ZVS is proposed in [10] and the maximum efficiency is reported as 70%. An improved version that uses dual-transistor flyback converter is proposed in [11] with the maximum efficiency of 86.7%. In [12], a flyback converter based on continuous conduction mode (CCM) is proposed and the weighted efficiency is obtained as 87.4%. The efficiency of the three-port flyback PV microinverter proposed in [13] is 90.6%. In [14], active clamp circuit and synchronous rectifier are utilized and the improved weighted efficiency is 95.1% at full load. The effect of DCM-BCM operation is analyzed in [15] to increase efficiency of the flyback microinverter. A hybrid switching method is used in [16] with an adaptive snubber and the peak efficiency is 95.8% for a 250-W prototype. Another hybrid method is proposed in [17] with 91% peak efficiency.

According to our literature review, the state of art efficiency for flyback-based inverters at 250 W is 95.8%, which relies on using hybrid switching method and an adaptive snubber. We have not come across any design that achieves such a high efficiency at much higher power. A flyback-based PV inverter presented in [18] achieves 90.16% efficiency at 2 kW. Likewise, [19] presents the same topology at 2.5 kW with an efficiency of 92.47%. Therefore, the objective of this research is to develop the highest-efficiency flyback inverter at the highest power ever reported in the literature. This study also develops a commercially competitive inverter by reducing the size and the cost. Figure 1 shows the schematic of the proposed grid-connected PV inverter based on three-cell interleaved flyback converter topology. It is also the model used in the simulation studies.

In order to accomplish the efficiency objective, the whole design including power stage, gate drive, and transformers was optimized to accommodate the use of the fastest switching devices such as silicon carbides (SiCs) without any setbacks. Since the leakage inductance is generally the major setback in the overall performance of any flyback-based converter, we put the major emphasize on the development and the design of flyback transformer. At the end of the study, a state-of-the-art flyback transformer with ultrahigh efficiency and practically the lowest leakage inductance is implemented. Besides bringing the efficiency to the top level, this research also builds a prototype that is very close to the final product so that a true cost and size analysis can be done to demonstrate the commercial value. For this purpose, five power devices with the fastest switching speeds are selected and tested to evaluate the performance versus the cost. These tests are first performed with silicon-IGBTs obtained from three different manufacturers to determine the benchmark. Then, two SiC MOSFETs with different electrical characteristics are tested to assess the contribution of silicon carbide technology to the efficiency. Later, the total cost is evaluated for each selected switching device, and a cost versus performance graph is obtained to help the designer to make the best compromise.

2. Analysis of the inverter

This section presents the major equations used in the design of the inverter in DCM operation. The detailed analysis of the converter can be found in the references provided. The relationship between the active power delivered by a PV source and the power transferred to the grid assuming unity power factor is the following.

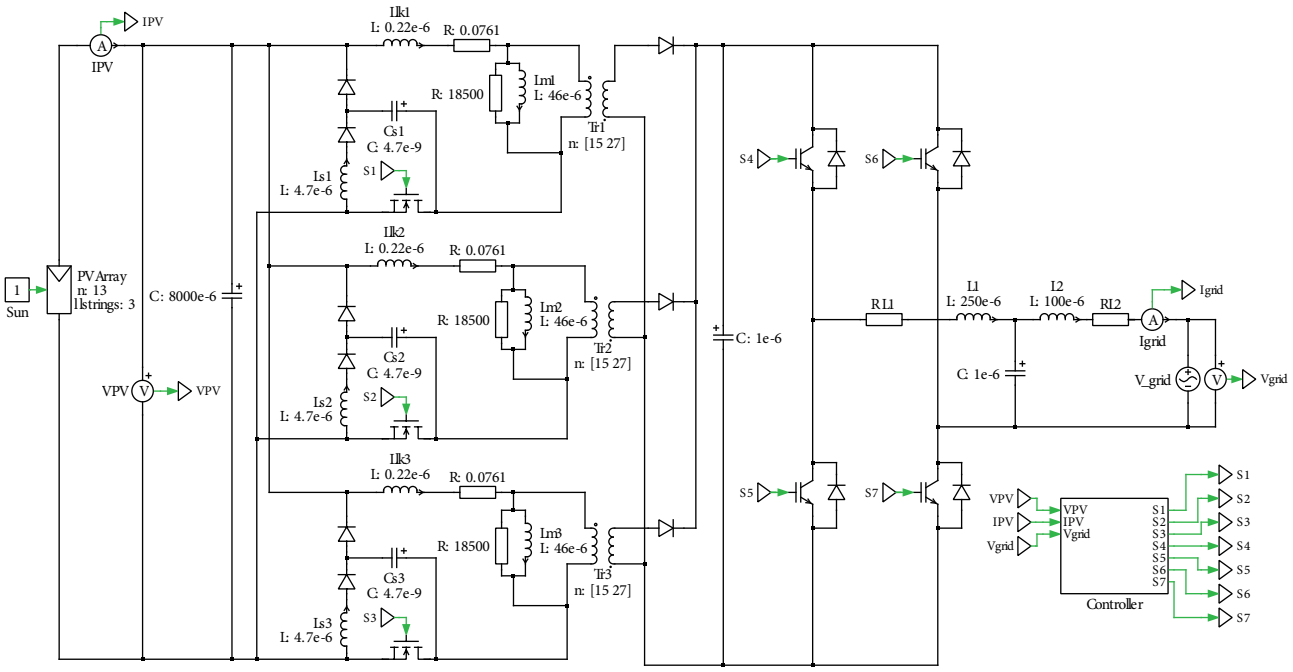


Figure 1. PLECS model of the proposed PV inverter.

$$P_{PV} = V_{PV} I_{PV} = \frac{n_{cell} V_{PV}^2 D_{peak}^2}{4 L_m f_s} = \frac{\hat{V}_{grid} \hat{I}_{grid}}{2} = P_{grid}, \tag{1}$$

where V_{PV} and I_{PV} are the average PV voltage and current at the maximum power point (MPP), n_{cell} is the number of flyback cells to be interleaved, L_m is the magnetizing inductance of the flyback transformer, and f_s is the switching frequency. Moreover, D_{peak} is the peak duty ratio determined by the maximum power point tracking (MPPT) algorithm occurring at the instant that the grid voltage is at its peak value ($\hat{V}_{grid}$). After L_m is determined, the flyback transformer turns ratio (n) is calculated as below.

$$n = \frac{\hat{V}_{grid}(0.9 - D_{peak})}{V_{PV} D_{peak}}. \tag{2}$$

The selection of n is very critical for the intended operation of the inverter. Therefore, in order to guarantee DCM operation, the value of V_{PV} at the MPP and the specified minimum value of the grid voltage ($\hat{V}_{grid}$) should be used in above equation. The number of primary turns is computed by using the desired maximum flux density ($B_{\max}$) and cross sectional area of the selected core (A_{core}) as follows.

$$N = \frac{V_{PV} D_{peak}}{f_s B_{max} A_{core}}. \tag{3}$$

The air gap length of the flyback transformer is determined as below.

$$l_g = \frac{N^2 \mu_0 A_{core}}{L_m}. \tag{4}$$

The utilization of solar energy from the panels and the THD of grid current is adversely affected by the voltage ripple. Therefore, the correct sizing of the decoupling capacitor is very important to achieve high inverter performance. The minimum value of this capacitor is calculated by using the average PV current and the peak-to-peak ripple (ΔV_{PV}) across the PV terminals as follows.

$$C \geq \frac{2I_{PV}}{(2\pi 100)\Delta V_{PV}}. \tag{5}$$

3. Power loss analysis

This section presents the analytical analysis of power losses in the inverter in order to estimate the theoretical efficiency in advance so that we can optimize the design for the best efficiency. First, we are going to describe the calculation of the losses in the switches. Thanks to operation in DCM, there are no turn-on losses in the flyback switches. Only conduction and turn-off losses are concerned. The conduction losses are calculated as below.

$$P_{conduction} = I^2_{sw_RMS} R_{DS(ON)}. \tag{6}$$

The peak turn-off losses are calculated as below.

$$P_{pk_turn_off} = \frac{1}{2}\hat{V}_{sw}\hat{I}_{sw}t_f f_s. \tag{7}$$

Eq. (7) gives only the peak losses because they occur at the peak of grid voltage ($\hat{V}_{grid}$) when both $\hat{V}_{sw}$ and $\hat{I}_{sw}$ have their largest values. Assuming the leakage inductance is zero, the peak voltage across the switch at that instant is found as follows.

$$\hat{V}_{sw} = V_{PV} + \frac{\hat{V}_{grid}}{n}. \tag{8}$$

Moreover, due to DCM operation, the peak of the current pulses follows a sinusoidal trajectory because of the sinusoidal modulation of the duty ratio. Thus, $\hat{I}_{sw}$ in Eq. (7) is the peak of the largest triangular current pulse that flows through the switch and calculated as below.

$$\hat{I}_{sw} = \frac{V_{PV} D_{peak}}{L_m f_s}. \tag{9}$$

Finally, the average turn-off losses over one grid cycle assuming that the profile of the losses in every switching instant follows a sinusoidal trajectory are calculated as below.

$$P_{avg_turn_off} = \frac{2P_{pk_turn_off}}{\pi}. \tag{10}$$

Because of DCM operation, there are no reverse recovery problems associated with the secondary side diodes. Only conduction losses are concerned. To determine the conduction losses, we have modeled the secondary side diodes with a series DC voltage source (V_{t0}) representing zero-current forward voltage and a resistance (r_d). The parameters V_{t0} and r_d are given in the datasheet for the selected diode. With this model, the expression of the conduction losses is as follows.

$$P_{D_conduction} = V_{t0} I_{F_avg} + r_d I^2_{F_RMS}, \tag{11}$$

where the parameters I_{F_avg} and I_{F_RMS} are the forward average and the RMS currents in the diode.

The switching losses of the unfolding H-bridge is negligible since the IGBTs are operated at the grid frequency. Therefore, only conduction losses are considered. An IGBT approximation with a series connection of DC voltage source (V_{CE0}) representing IGBT on-state zero-current collector-emitter voltage and a collector emitter on-state resistance (R_{CE}) is used to determine the conduction losses as below.

$$P_{IGBT_conduction} = V_{CE0} I_{CE_avg} + R_{CE} I^2_{CE_RMS}. \tag{12}$$

In order to determine the core losses, we should first find the core loss density using the formula given below.

$$P_{core_loss_density} = C_m f^a B^b (c_{to} - c_{t1} T + c_{t2} T^2), \tag{13}$$

where C_m, a, b, c_{to}, c_{t1}, and c_{t2} are the parameters which have been found by curve fitting of the measured core loss data, f is frequency (Hz), B is the flux density (T), and T is temperature (°C). The result is found in mW/cm^3. We should note that the flux density B in Eq. (13) is not constant in our application. It rather changes in a profile that follows a sinusoidal path since the duty ratio is modulated sinusoidally. Therefore, the peak of that path, which is calculated as below, used in Eq. (13) to calculate the peak core loss density.

$$\Delta B = 2B_{peak} = \frac{V_{PV} D_{peak}}{N f_s A_{core}} \tag{14}$$

The average core losses over one grid cycle can be calculated by multiplying P_{pk_cld} by the effective core volume (V_e) as follows.

$$P_{core} = \frac{2(P_{pk_cld} V_e)}{\pi}. \tag{15}$$

Since our primary objective was to increase efficiency and reduce the leakage inductance both at the same time, we used copper foils for the windings. Therefore, the following analysis was done to define the losses for the windings. The resistance of a winding made with copper foil was found as.

$$R_w = \frac{\rho l_s}{d_s b_s} N, \tag{16}$$

where ρ is the resistivity (Ωm), l_s is the mean length turn, d_s is the thickness of the foil, b_s is the winding breadth and N is the number of turns. Comparing the thickness of the foil (0.03 mm) with the skin depth of copper at 40 kHz, which is 0.38 mm, eddy current losses can be neglected.

It is not possible to make the leakage inductance zero, but our aim is to achieve the lowest inductance practically possible. We are targeting an inductance value that is less than 0.5% of magnetizing inductance. The following formula finds the losses over one grid cycle due to the leakage inductance assuming all the energy in the leakage is dissipated in the flyback switch.

$$P_{Llk_loss} = \frac{L_{lk} \hat{I}^2_{pri} f_s}{\pi}. \tag{17}$$

4. Design of inverter

The main objective of this research is to design an isolated PV inverter with high efficiency for residential applications. Based on our market research, we have discovered several commercial PV inverters that fall

within our intended application. The specifications listed in Table 1 are determined in a way that the proposed design yields a commercially competitive inverter. Since the most important design criterion is the efficiency, almost all the design decisions including component and parameter selections are made based on the expected efficiency increase.

Table 1. Design specifications of the proposed PV inverter.

Design parameters	Specifications
Selected PV model and maximum power	BP365, 65 W
OC voltage and SC current per panel	21.7 V, 3.99 A
Voltage and current at MPP per panel and per panel group (13S3P)	17.60 V, 3.6932 A, 228.80 V, 11.0796 A
Maximum DC power from PV panel system	2535 W
Selected MPPT voltage range	175 V – 300 V
Maximum input voltage	350 V
MPPT energy harvesting efficiency	>99%
Inverter efficiency	>95%
Grid characteristics	230 V, Single-phase, 180 V – 264 V_{RMS}
Grid current %THD	<4%
Power factor	>0.99
Switching frequency	40 kHz
Number of interleaved cells	3 cells

As the first step, we developed a power flow chart as seen in Figure 2, which shows the maximum allocated power losses for each major component of the inverter. These allocations yield 125.5 W total losses and allow a design that can achieve a minimum efficiency of 95%. In order to supply 2535 W power, 65-W panels are used in 13S3P arrangement, where 13 panels are connected in series to form a string and 3 strings are connected in parallel. Assuming 99% efficiency for MPPT algorithm, available input power becomes 2510 W for the inverter. As long as we can realize the losses given in the chart during the design stage, we can reach our goal easily. The calculation of losses for each component is provided in the following subsections.



Figure 2. Power flowchart of the proposed inverter.

Another improvement that contributes to the overall efficiency compared to our past work is the increase of the input voltage, since the effective value of the input current decreases in the same proportion. Moreover, a lossless resonant turn-off snubber described in [20] is employed to suppress the over voltages at switch turn-offs but also to reduce the turn-off switching losses.

4.1. Design of flyback transformer

Due to three-cell interleaving, the theoretical value of D_{peak} is equal to $1/n_{cell} = 1/3$, but a slightly larger value is used to get a practical number for magnetizing inductance L_m. Therefore, using $D_{peak} = 0.345$,

$V_{PV} = 228.8\ V$, $P_{PV} = 2535\ W$, and $f_s = 40\ kHz$ in Eq. (1), we determined the magnetizing inductance as $L_m = 46\ \mu H$. Moreover, using $\hat{V}_{grid} = \sqrt{2} \times 180\ V$ in Eq. (2), we calculated the minimum value of the turns ratio as 1.793, which guarantees DCM operation. Next, we selected a core that would provide significantly low core losses and allow a compact transformer design with less magnetic radiation. The PM 87/70 part numbered ferrite core made by Ferroxcube with 910 mm^2 cross-sectional area is selected for this purpose. Using the nominal values of D_{peak}, V_{PV}, f_s, and A_{core} with $2B_{max} = 0.15\ T$ in Eq. (3), we have calculated the number of primary turns as 14.44 and rounded to 15. Hence, the number of the secondary turns becomes 27 since the turns ratio is 1.8. Using the circuit parameters in Eq. (14), B_{peak} is found as 0.0723 T. Then, using the 3C90 core material coefficients given in reference [21], $C_m = 3.2 \times 10^{-3}$, $c_{t0} = 2.45$, $c_{t1} = 3.1 \times 10^{-2}$, $c_{t2} = 1.65 \times 10^{-4}$, $a = 1.46$, $b = 2.75$, 40 kHz for f, 0.0723 T for B, and $100°C$ for T in Eq. (13), the peak core loss density is calculated as 12.21 mW/cm^3. Multiplying this number by $V_e = 133\ cm^3$ for the selected core and using it in Eq. (15), the average core loss is found as 1.03 W. As expected, this loss is quite low.

In order to achieve the maximum coupling and practically the lowest leakage inductance, we used the sandwich winding strategy where both primary and secondary windings are sectionalized into three parts and then interleaved to construct three-layer sandwich windings, effectively reducing the magnetic field in the window area. Additionally, the windings are made using copper strips so that practically the most compact coil with the lowest height can be achieved. A great effort has gone into the preparing of the windings. If not done properly, large extra spaces are created between the windings and the turns during the step that the three sections are connected in series. In addition, if you are using wide copper strips for winding, it is much harder to run the conductors inside the transformer. If these extra spaces are not avoided by using the proper techniques, very large amount of leakage inductance is inevitable. In this design, after many trials, the optimum folding points and folding angels, and the lead placement points are determined, then the coils are wound and practically the best-coupled coils are realized. The compact design of windings also contributes to the low winding losses. For primary winding, using $\rho = 2.26 \times 10^{-8}\ \Omega m$, $l_s = 11.8 \times 10^{-2}$ m, $d_s = 3 \times 10^{-5}$ m, $b_s = 32 \times 10^{-3}$ m, and $N = 15$ in Eq. (16), winding resistance is found as 0.0417 Ω. Since the primary RMS current is 9.25 A, the copper loss for the primary winding is found as $P_{copper_pri} = (9.25)^2(0.0417) = 3.568$ W. For secondary winding, using $l_s = 12.1 \times 10^{-2}$ m and $N = 27$ in Eq. (16), winding resistance is found as 0.0769 Ω. Since the secondary RMS current is 6.535 A, the copper losses for the secondary winding are calculated as $P_{copper_sec} = (6.535)^2(0.0769) = 3.284$ W. Therefore, the total core and winding losses are 7.88 W for one flyback transformer and 23.65 W for three transformers. This number is 0.942% of input power, which is less than our 1% allocation. Lastly, the air gap length is calculated as 5.593 mm by using Eq. (4). The air gap is then divided into 6 sections that are distributed along the center leg to minimize both the fringing flux and the leakage flux. Figure 3 shows the selected core, the sliced center leg, the finished coil, the air gap materials, and the finished flyback transformer. The magnetizing inductance measures 46 μH as designed and the leakage inductance measures as 220 nH. This value corresponds to 0.47% of the magnetizing inductance, proving the effectiveness of our design method. Due to this accomplishment, it is possible to operate the inverter even under hard switching or reduce the snubber size significantly. Realization of small leakage is also very favorable for efficiency. Using $L_{lk} = 0.22\ \mu H$ and $\hat{I}_{pri} = 42.9$ A in Eq. (17), the losses due to the leakage inductance of three transformers are calculated as 16.17 W. This correspond to 0.64% of input power if they are not recovered by snubber circuit.

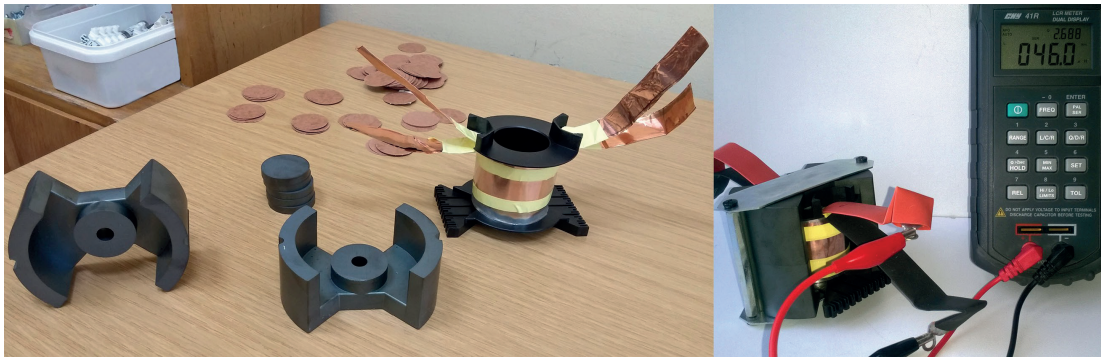


Figure 3. PM87/70 ferrite core set, the sliced center leg, the finished coil and flyback transformer.

4.2. Design of power stage

Power stage design starts with sizing of the decoupling capacitor. It controls the voltage ripple at the PV terminals. Based on our earlier experience, the THD of the grid current is lower and the energy utilization performance of MPPT is better if the voltage ripple is small. Based on simulation studies, 2% ripple corresponding to 4.58 V is determined as the best compromise between the performance and the size. Then, using Eq. (5) we have calculated the optimum value of the decoupling capacitor as 7700 μF.

Next step involves selection of switching elements. The maximum voltage stress is 557 V for the primary side switches and 1003 V for the secondary side diodes making 1200 V rated devices suitable for both. In addition, the unfolding bridge will use 600 V rated devices since they are subjected to the grid only. In order to realize our efficiency objective, the C2M0025120D part numbered SiC MOSFET made by Cree is selected as the primary side switch. Using $R_{DS(ON)} = 43$ mΩ (worst-case) and $I_{RMS} = 9.25$ A (it is obtained from simulation) in Eq. (6) the conduction losses for the selected switch are calculated as 3.68 W. Again, using $V_{PV} = 228.8$ V, $\hat{V}_{grid} = \sqrt{2} \times 230\ V$, and $n = 1.8$ in Eq. (8), $\hat{V}_{sw}$ is calculated as 409.5 V. Then, using $D_{peak} = 0.345$, $L_m = 46$ μH, and $f_s = 40$ kHz in Eq. (9), $\hat{I}_{sw}$ is calculated as 42.9 A. Finally, using $t_f = 52\ ns$ in Eq. (7), $P_{pk_turn_off}$ is found as 18.27 W, and using this peak power in Eq. (10), $P_{avg_turn_off}$ is calculated as 11.63 W. Therefore, the total losses for three flyback switches are calculated as 45.93 W, corresponding to 1.83% of total input power. This number is less than our 2% allocation.

The SCS215KGC part numbered SiC Schottky diode by Rohm is selected as the secondary side diode. Using $V_{t0} = 0.82$ V, $I_{F_avg} = 3.31$ A, $r_d = 0.057\ \Omega$, and $I_{F_RMS} = 6.54$ A (obtained from simulation) in Eq. (11), the conduction losses for the selected diode are calculated as 5.15 W. The total loss for three diodes at the output are calculated as 15.45 W, corresponding to 0.615% of total input power. This number is little bit higher than 0.5% allocation. The IKW75N60T part numbered IGBT by Infineon is selected for the unfolding H-Bridge. Using $V_{CE0} = 0.45$ V, $I_{CE_avg} = 4.96$ A, $R_{CE} = 0.04\ \Omega$, and $I_{CE_RMS} = 7.79$ A in Eq. (12), the conduction losses are calculated as 18.65 W for four IGBTs in the bridge. The total losses correspond to 0.743% of input power. This number is lower than our 1% allocation. In the final step, the output filter is sized. This design utilizes an LCL filter since it provides higher power quality [22]. After the optimum cut-off frequency of the filter is determined as 18.83 kHz via simulation, the filter elements are determined as shown in Figure 1.

4.3. Control system

The control system has the capability of harvesting the maximum power from the panels by using perturb and observe (P&O) MPPT algorithm and simultaneously injecting the collected solar power into the grid with high

power quality. The peak duty ratio (D_{peak}) produced by the MPPT algorithm is multiplied by the PLL output in order to produce the reference signal to synthesize a current in phase with the grid voltage. Since the flyback cells are interleaved, control of each flyback cell is phase-shifted with respect to each other. The PLL output signal is also used for the sequencing of the switches in the unfolding bridge. One can refer to [18] for more in-depth discussion about the control system.

Since the flyback cells are interleaved, control of each flyback cell is phase-shifted with respect to each other as shown in Figure 4a. The control signal generated by the MPPT algorithm for each cell is the same but the carrier waveforms are phase shifted by 120°. The phase-shifted switching pattern and the primary currents of the interleaved flyback cells, and the total primary current is shown in Figure 4b. The PLL output signal is also used for the sequencing of the switches in the unfolding bridge. The complete control system has been implemented in Texas Instruments TMS320F28335 DSP controller.

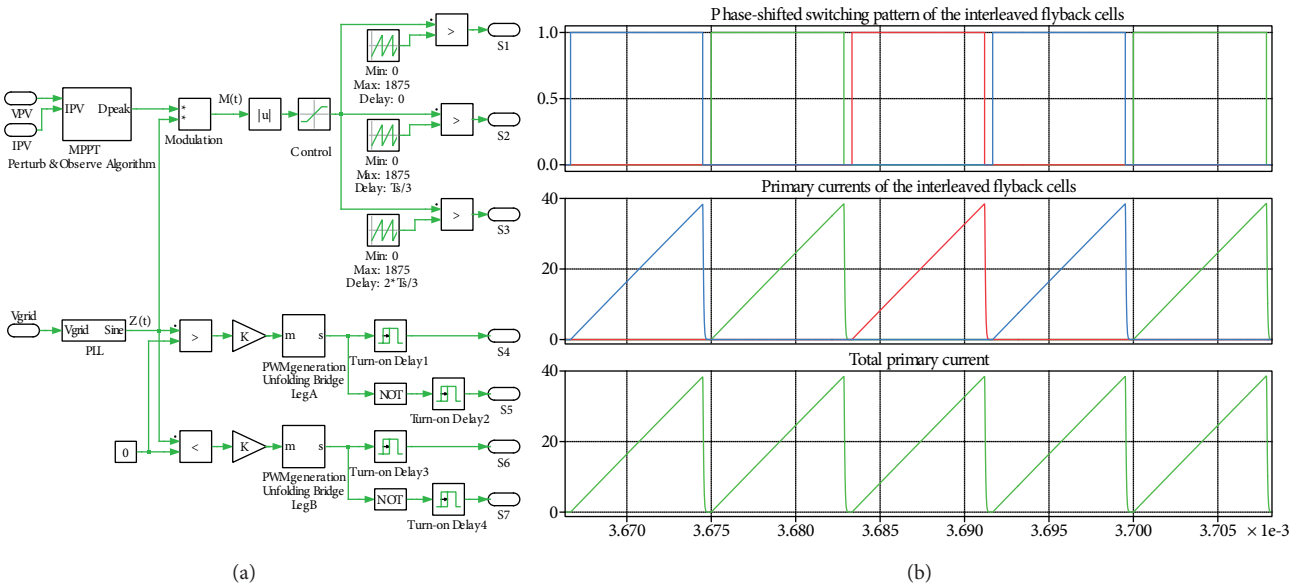


Figure 4. a) Control system, b) Phase-shifted switching pattern, primary currents of interleaved cells (green - cell 1, blue - cell 2, red - cell 3), and total primary current.

The current sharing is achieved naturally among the phase-shifted cells because of the employed control system. In DCM method with open loop control, the magnitude of the current is determined by the MPPT controller; and the shape and phase of the current is controlled by the PLL output. Contrary to the continuous current mode of operation (CCM), there is no need for any current control loop that requires the instantaneous regulation of the output current. In CCM operation, each cell current must be measured and regulated for equal current sharing. Therefore, this is the major advantage of DCM operation with open loop control.

5. Simulation results

Simulation has been the key tool for the optimization of the current design for the best efficiency. The part of the components that contribute to the power losses are determined and modeled in the PLECS simulation circuit as shown in Figure 1. Therefore, all of the analytical calculations are verified for all operating conditions. Based on the simulation results, the theoretical maximum efficiency of the inverter has been determined as 95.26% under hard switching and 95.88% under soft switching. The hard switched efficiency is slightly above the specification.

In order to guarantee high efficiency in experimental prototype, we decided to use a losses turn-off snubber to recover the energy in leakage inductance also reduce the turn-off losses. With an optimum design of snubber, we expect to bring the practical efficiency closer to the theoretical maximum. In addition, Figure 5 shows three sun radiation levels along with the output power of the PV panels and the power delivered to the grid under hard switching. It shows that the MPPT algorithm successfully tracks the changes and yields 99% efficiency for all radiation levels.

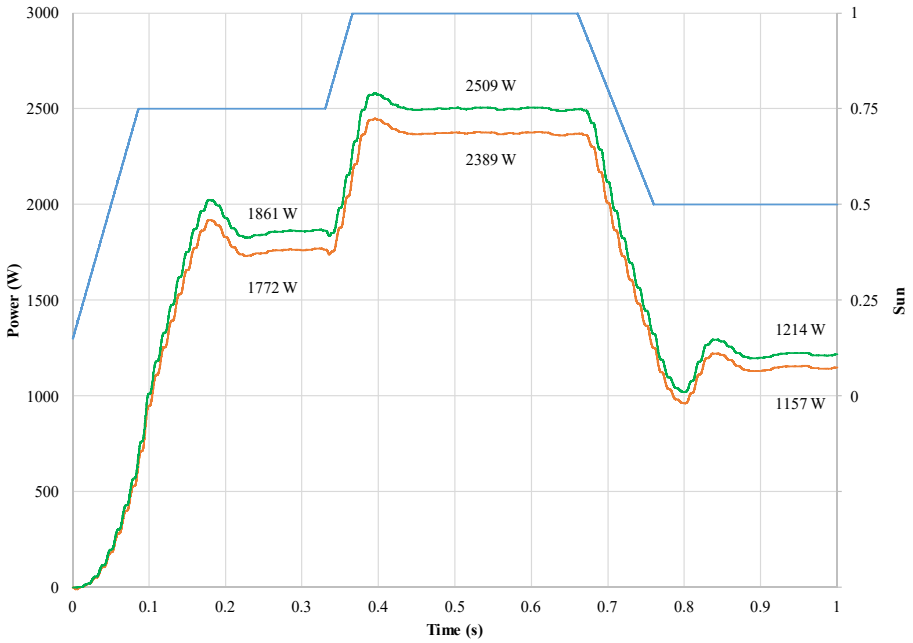


Figure 5. Three different sun radiation levels (blue) with PV output power (green) and power delivered to the grid (orange).

6. Optimizations and experimental results

A prototype circuit at 2.5 kW rated power is built as shown in Figure 6. The HDO4034 LeCroy oscilloscope is used for waveform capturing and the Hioki 3193 is used for power quality analysis. Before the tests, we spent a great amount time and effort to optimize the hardware for the best overall performance.

6.1. Optimizations

Since the priority was to increase the efficiency, we selected the highest-efficiency switching devices available from several manufacturers. These devices also come with the highest switching speeds that is hard to handle in a flyback-based converter. The major difficulties are elimination of noise, keeping the devices in their safe operating area, and designing of an efficient gate driver for each device especially for the SiC MOSFETs. Consequently, it took great effort and time to solve each problem effectively.

The selected SiC MOSFETs have the maximum gate-to-source voltage rating of +25 V/−10 V specified by the manufacturer. It is also recommended by the manufacturer that the gate voltage swing should be close to +20 V/−5 V in order to get the best switching performance. Considering the high speed of the devices, this is a small safety margin; therefore, the transient overshoots must be closely monitored and suppressed. As the first obvious precaution, the parasitic inductances are minimized at the gate drive circuit. Then, the

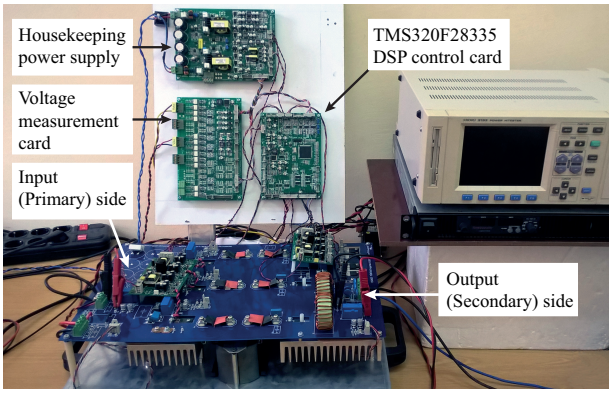


Figure 6. Prototype of the three-cell interleaved 2.5 kW flyback PV inverter.

optimum value of the gate resistance is determined. One thing we observed is that the increasing of the gate resistance affects the efficiency badly but does not reduce the transients at the same ratio. After many test and trials, 4.7 Ohm is selected as the best compromise between efficiency and the overshoot values. Although everything that is physically possible was tried, we had to place a 1-nF capacitor between the gate and source pins of the SiC MOSFETs to limit both the positive and negative overshoots. In our case, the capacitor is more effective than increasing the value of the gate resistance. We also placed TVS diodes LCE20A from Littelfuse and 1N5908G from ON semiconductor between these pins as an extra safety measure. Note that the 1-nF capacitor is not used with the IGBTs.

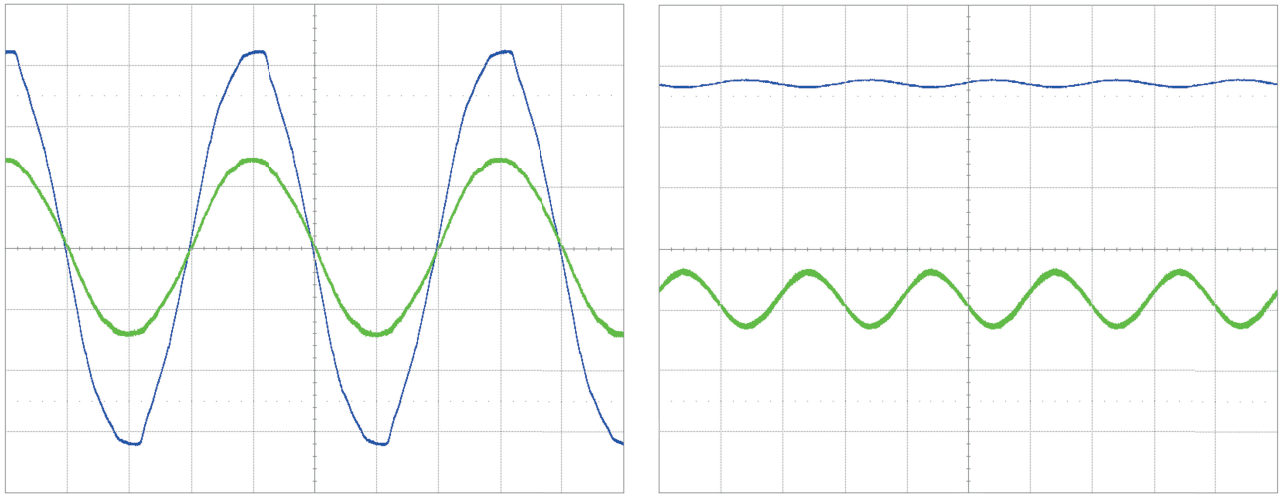
In addition, the snubber circuit is optimized for the best efficiency rather than voltage suppression purpose since the leakage inductance is already minimized in large extent. The highest efficiency with low transient voltage overshoots is achieved with 4.7-nF snubber capacitor and $4.7-\mu$H snubber inductor. Note that higher capacitor values yield more suppression of transient overshoots but the efficiency begins to decrease because the energy circulating in the nonideal snubber components becomes excessive.

We also put major emphasis on the design of the PCB to achieve the most efficient and compact layout with the lowest parasitic elements. Low resistive paths are created for high-RMS currents by employing wide and $200-\mu$m thick copper traces. Both the primary and secondary side circuits of the flyback inverter are placed on a single PCB to achieve a smaller footprint. The flyback transformer terminals, which are also made of copper strips, are connected to PCB via terminal blocks that have the largest contact area possible.

6.2. Test results

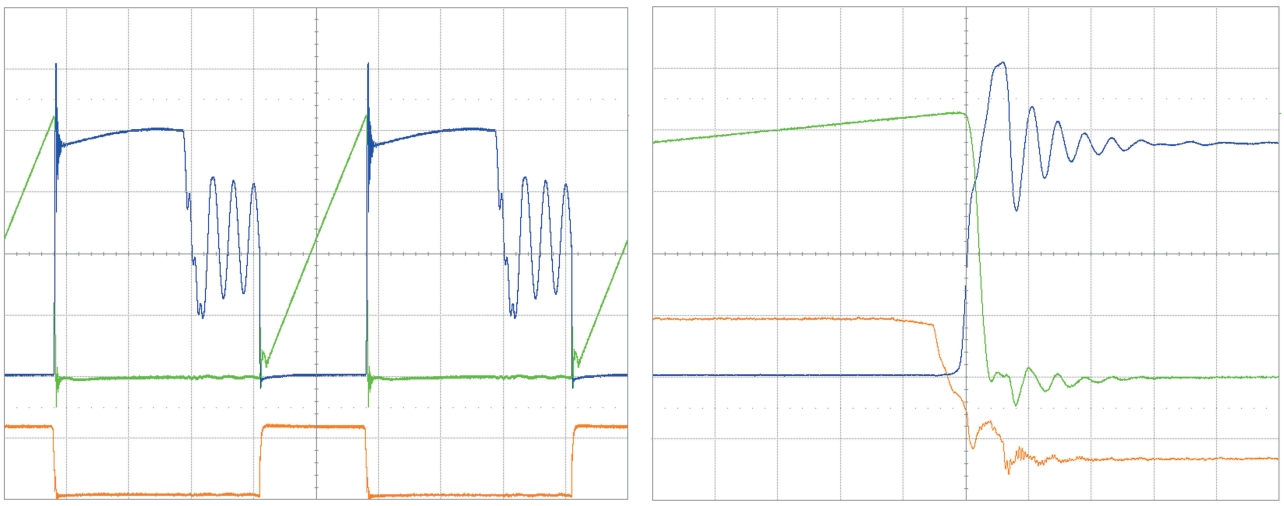
Figure 7a shows the waveforms of the grid voltage and current when SiC MOSFET C2M0025120D is used. The waveforms confirm the high power quality interface to the grid. The power factor is measured close to unity and the THD of the grid current is measured as 1.73% at rated power. The increase of input voltage from 88 V to 228.80 V significantly improves the THD from 4.42% to 1.73%. This improvement is due to the reduced voltage ripple since the current ripple through the decoupling capacitor is also reduced in the same proportion. Figure 7b shows the measured PV voltage and PV current waveforms recorded during the same test. The ripple across the PV terminals is measured as 5.67 V, which is slightly higher than expected (4.58 V). The new design achieves much better THD of the grid current with smaller decoupling capacitor. Figure 8 shows the waveforms of the gate signal, the voltage across, and current through the switch and the close-up view of the same waveforms at the turn-off instant. The peak current is 42.52 A and the peak switch voltage

is 510 V with an overshoot less than 30% at the worst case, confirming that flyback transformer has very low leakage inductance and snubber circuit performs well.



(a) (b)

Figure 7. a) Grid voltage (blue) (100 V/div) and grid current (green) (10 A/div), b) PV voltage (blue) (40 V/div) and PV current (green) (5 A/div) (Time: 5 ms/div).

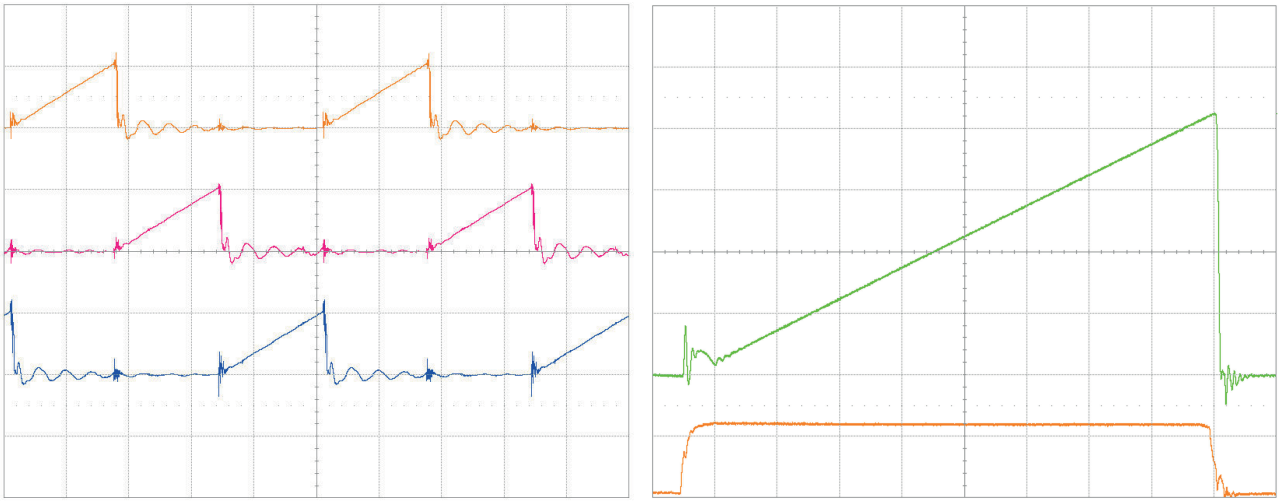


(a) (b)

Figure 8. a) MOSFET voltage (blue) (100 V/div), current (green) (10 A/div) and gate signal (orange) (Time-axis: 5 μs/div), b) Closer view of the same waveforms at the turn-off instant (Time-axis: 200 ns/div).

Figure 9a shows the primary side current of each flyback cell. The waveforms indicate the 120° phase-shifted operation. It is obvious that when these currents add up at the point of common coupling, there will be almost no discontinuity and the ripple frequency at the PV current will be three times the switching frequency. The result of interleaving, as demonstrated here, is the easy filtering of the high frequency harmonics and obtaining high quality waveforms at the PV side as well as at the grid side. Only cell 1 is made available for probe measurement. For this reason, the combined measurements of three cell currents were done using current

sensors. The noise and the oscillations around the waveforms are due to the wiring inductance. When a current probe is used no oscillations are observed as shown in Figure 9b. Figure 9b shows the converter primary current and the gate signal, verifying the successful DCM operation. The bump in the current at the beginning of the cycle demonstrates that the snubber is working effectively. This small bump is expected because of the operating principle of the turn-off snubber indicating that the resetting mechanism is working efficiently and getting the snubber ready for the next turn-off. Since the flyback MOSFET is within the snubber current loop, this bump appears only on the drain current for a short time which has no considerable effect on the efficiency.



(a) (b)

Figure 9. a) Primary side current of each flyback cell (40 A/div) (Time-axis: 5 μs/div), b) Converter primary current (green) (10 A/div) and gate signal (orange) (20 V/div) (Time-axis: 1 μs/div).

Figure 10a shows the measured efficiencies for five devices and for the loading conditions that correspond to four different sun radiation levels. The maximum efficiency of the inverter is measured as 95.82% with Cree SiC MOSFET C2M0025120D at 75% load, which is almost equal to the simulated efficiency. It yields 95.35% at 25% load and 95.60% at full load. These numbers are well above our design specification of 95% for wide load range. The best performance is obtained with this device since it has the fastest turn-off speed and low $R_{DS(ON)}$ resistance (25 mΩ). The second best device is again a SiC MOSFET from Cree (C2M0080120D) and it has $R_{DS(ON)} = 80$ $m\Omega$. This device achieves an efficiency of 95.06% at 25% load and 94.91% at full load. These numbers suggest that the second Cree device satisfies our design specification as well. As far as the Silicon IGBTs, the Microsemi IGBT (APT45GP120BG) has the best performance with 93.92% efficiency. The Fairchild IGBT (FGH40T120SMD) follows it with 92.58% and lastly the IXYS IGBT (IXYH50N120C3) achieves 92.42%. It can be concluded that the superior switching characteristics give SiC MOSFETs a true advantage in terms of efficiency as long as the gate voltage requirements are fulfilled and transient overvoltages across the gate terminals are kept within the safe limits.

These results clearly demonstrate that the proposed design greatly enhances the efficiency compared with the past work. Therefore, the 95.82% efficiency is the state-of-the-art efficiency for flyback based grid-tied PV inverters at 2.5 kW ever reported in the literature. The maximum efficiency of the flyback converter stage alone reaches 96.50% when we exclude the IGBT conduction losses of the unfolding H-bridge. Based on these results, we can conclude that the implementation of three-cell interleaved flyback inverter at 2.5 kW with high

efficiency is practical, and our research objective is achieved successfully.

6.3. Cost and size analysis

For the cost analysis, we have obtained the component prices from Digi-Key and Mouser Electronics based on the listed prices of 1000 quantity. Some inductors are purchased from CoilCraft Inc., and flyback transformers and few other components are provided by the local manufacturers. We have determined the total component cost as $680.35. Although we think it is highly possible to reduce the cost further down, this is still low enough to produce a highly competitive commercial product. Figure 10b shows the change of cost versus the efficiency at rated power for five power semiconductors evaluated in this study. As it is expected, the Cree MOSFET C2M0025120D has the highest cost but yields the highest efficiency. The Fairchild IGBT FGH40T120SMD has higher efficiency but lower cost than the IXYS IGBT IXYH50N120C3. In this study, the Cree MOSFET C2M0080120D has the best compromise between the performance and the cost.

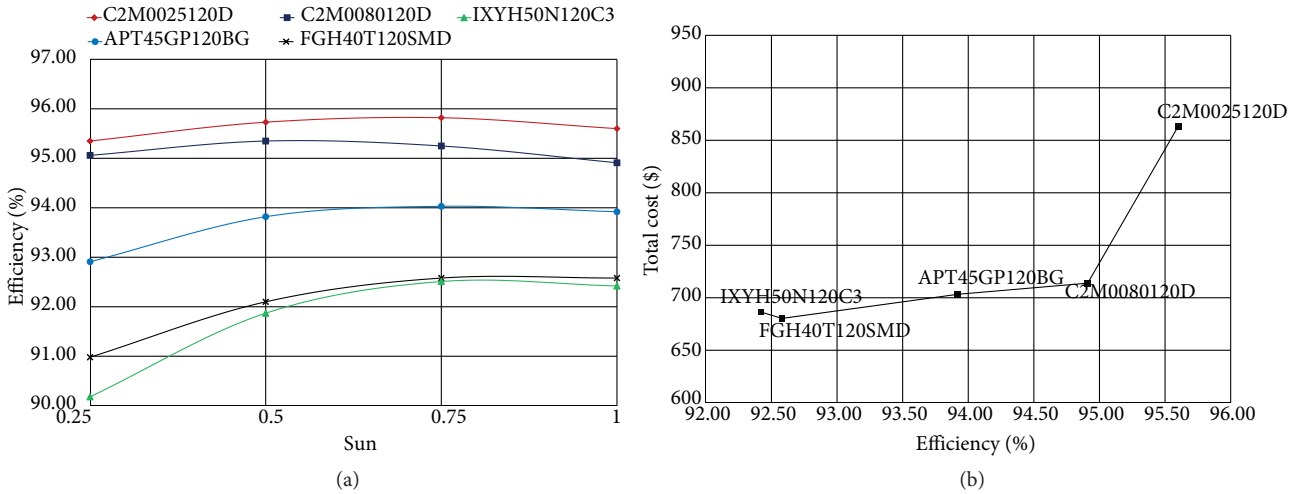


Figure 10. a) Measured efficiencies for five devices versus four loading conditions, b) Total cost versus efficiency at nominal power for five switches.

The dimensions of the current prototype shown in Figure 6 are 345 × 520 × 165 mm. This is truly a compact inverter compared to the similar products in the market. Nevertheless, there are still extra spaces to get rid of. Finally, the total weight of the inverter is 15 kg. The comparison results are presented in Table 2.

Table 2. Cost and size comparison.

The inverter	Sunny Boy 2500HF-30 (SMA)	UNO 2.5-I-OUTD (ABB)	Proposed inverter
Dimensions (mm)	348 × 580 × 145	367 × 518 × 161	345 × 520 × 165
Weight (kg)	17	< 17	15
Price ($)	2538 (selling price)	2564 (selling price)	680.35 (component cost)

7. Conclusions

A grid-tied and isolated PV inverter based on the interleaved flyback converter topology rated at 2.5 kW has been implemented with 95.82% maximum efficiency. This is the highest efficiency ever reported in the literature

for such a high-power flyback inverter operated in DCM. The main contribution of this study is the achievement of a challenging design objective. Moreover, the results will change the perception in favor of the flyback topology in inverter designs where galvanic isolation in kilowatt range is desired. Consequently, the research has produced a commercially viable and competitive inverter for small power and residential photovoltaic applications.

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