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High-temperature sensitivity complex dielectric/electric modulus, loss tangent, and AC conductivity in Au/(S:DLC)/p-Si (MIS) structures

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ABSTRACT

Complex dielectric ($\varepsilon^* = \varepsilon' - j\varepsilon''$)/electric modulus ($M^* = M' + jM''$), loss tangent (tan$\delta$), and ac conductivity ($\sigma_{ac}$) properties of Au/(S-DLC)/p-Si structures were investigated by utilizing admittance/impedance measurements between 80 and 440 K at 0.1 and 0.5 MHz. Sulfur-doped diamond-like carbon (S:DLC) was used an interlayer at Au/p-Si interface utilizing electrodeposition method. The capacitance/conductance (C/G) or (ε' ~ C) and (ε'' ~ G) values found to be highly dependent on both frequency and temperature. The increase of them with temperatures was attributed to the thermal-activated electronic charges localized at interface states (N_{ss}) and decrease in bandgap energy of semiconductor. The observed high ε' and ε'' values at 0.1 MHz is the result of the space/dipole polarization and N_{ss}. Because the charges are at low frequencies, dipoles have sufficient time to rotation yourself in the direction of electric field and N_{ss} can easily follow the ac signal. Arrhenius plot (ln(σ_{ac}) vs 1/T) shows two distinctive linear parts and activation energy (E_a) value was found as 5.78 and 189.41 from the slope; this plot at 0.5 MHz is corresponding to low temperature (80–230 K) and high temperature (260–440 K), respectively. The observed higher E_a and ε' (~ 14 even at 100 kHz) show that hopping of electronic charges from traps to others is predominant charge transport mechanism and the prepared Au/(S:DLC)/p-Si structure can be used to store more energy.

1 Introduction

Metal–interlayer–semiconductor (MIS)-type Schottky contacts (SCs) are important electronic device for electronic industry as they are used in many applications, such as power electronics [1], solar cells [2], photodiodes [3], capacitors, and transistors [4]. They have more beneficial properties over P/N contacts like low signal-to-noise ratio, high power capacity, high rectification ratio (RR), and high-speed switching elements

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[5]. However, performance of these contacts are limited by work function and interface properties of metal and semiconductor. Studies on these structures have gained momentum with the observation of natural or artificially formed interlayer at metal/semiconductor interface that leads to an important change in the electric/dielectric properties of metal/interlayer/semiconductor (MIS)-type SCs [6, 7]. In many studies, to change and control the barrier height (BH), the performance of metal–semiconductor (MS) structure is improved usually using an organic or insulator interlayer. In other words, especially high dielectric organic compounds [7], polymers [8], nitride layers [9], metal oxides [10], and diamond-like carbon films [11, 12] have been used as an interlayer to increase the MIS-type SDs and capacitors.

Among these type of materials, diamond-like carbon (DLC) films are an important class of coating materials which have superior properties depending on the proportion of sp^2 and sp^3 bonds. The deposition method and doping are also the most important parameters that determine the bond structure [13–16]. These films are mostly deposited by chemical vapor deposition (CVD) and physical vapor deposition (PVD) methods for a wide variety of applications, as high-quality films can be obtained by these methods [13, 17, 18]. Another deposition method is the electrochemical deposition method which is very easy when compared to the others [11]. Relatively lower-quality films are obtained by the electrodeposition for mechanic and tri-biological applications. However, recently, our group have used the electrodeposited DLC films to fabricate MIS-type SDs. Well and encouraging results have been obtained by DC characterization of these devices [11, 12, 19]. So, AC characterization, frequency, and voltage dependence of the fabricated device are also important and require investigation to determine the applicability of the obtained devices. Dielectric materials are widely used in MIS/MOS capacitors and MISFET/MOSFET field-effect transistors because of their charge storage capabilities. Also, they are often used to improve the performance of semiconductor devices. Dielectrics can be easily polarized by an external electric field [20, 21]. Thus, dielectric acquires a net dipole moment. This is known as polarizability.

Today, the basic scientific/technical problems of the MS and MIS-type SCs is relevant to improve the performance of these structures and reduce the cost using new interfacial layer. Dielectric properties and conductivity in MIS-type structures depend on many factors, such as cleaning surface of semiconductor, interfacial layer thickness and its dielectric value, applied voltage, frequency, temperature, series resistance (R_s), surface states (N_{ss}) and their lifetimes (τ). In addition, for the analysis of their electric and dielectric measurements at only one frequency, temperature, voltage, or a narrow, these regimes cannot give more accuracy and reliable information to us on the basic electric/dielectric properties and conduction mechanisms.

Therefore, in the present work, sulfur-doped DLC (S-DLC) interfacial layer was grown onto p-Si wafer by electrodeposition technique using methanol as carbon source and thiophene as sulfur source. The morphology and chemical composition of the film have been analyzed using scanning electron microscopy (SEM) and X-Ray photoelectron spectroscopy (XPS), respectively. The obtained film on p-Si wafer has been used to perform an Au/(S-DLC)/p-Si device. In addition, dielectric permittivity, ac conductivity, and electric modulus were evaluated using the measured admittance data at two frequencies and over a wide temperature range.

2 Experimental detail

The nanocomposite film was deposited onto p-Si wafer by utilizing two-electrode electrodeposition setup. The electrolyte was prepared by mixing 100-ml methanol and 100-µl thiofuran. Graphite plate and p-Si substrate were used as anode and cathode, respectively. The distance between the electrodes, the applied potential, and duration time were 4 mm, 500 V and 2 h, respectively. More details on the deposition system were given elsewhere [11, 12]. SEM images of the FEI FEG-Quanta 450 model were caught. A SPECS photoelectron spectrometer with a monochromatic-AlKa X-Ray (XR) was utilized to manage the XR photoelectron spectroscopy investigation. To measure the admittance of the Au/S-DLC/p-Si device, HP-4192A LF impedance analyzer was used. In order to perform the C–V–T and G/ω-V-T measurements, the prepared device was placed into VPF-475 cryostat and then they were carried out between 80 and 440 K at 0.1-MHz and 0.5-MHz frequencies.

3 Results and discussion

3.1 SEM analysis

The SEM spectra of the (S-DLC) interlayer is shown in Fig. 1. Figure 1 shows that the Si wafer is fully covered by a continuous, crack-free, and lumpy film. In this study by changing the deposition parameters crack-free film could be obtained.

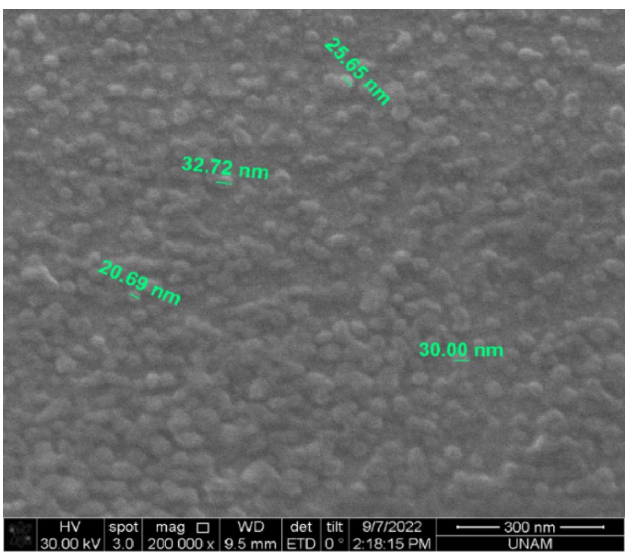

Fig. 1 SEM image of the prepared S-DLC film by utilizing electrodeposition method

3.2 XPS analysis

Figures 2a and b show the C 1s and S 2p XPS spectra of the S-DLC nanocomposite film. In Fig. 2a, C 1s spectrum was de-convoluted into three different peaks with different magnitude and binding energy which was attributed to C–S, C–C, and C–OOH, respectively [22]. Figure 2b shows that the S 2p spectrum appeared around 167.8 eV binding energy that was assigned to sulfide compounds (like C–S–C and H_2S) [12]. As can be clearly seen from the XPS spectra, the S has been thoroughly doped into the DLC film.

3.3 Admittance measurements

Admittance measurements of the fabricated Au/(S-doped DLC)/p-Si (MIS) are based on the voltage-dependent capacitance/conductance–voltage–temperature (C–V–T, G/ω–V–T) measurements of device for 01 and 0.5 MHz in a wide range of temperature (80–440 K) to obtain a detail information on the basic electric, dielectric, and conduction mechanism. Therefore, both the C–V and G/ω–V measurements type device/structure were carried out at between − 4 V and + 8 V as shown in Fig. 3a and b and Fig. 4a and b, respectively. As seen in these figures, as the temperature increases, the C value for all the frequencies increases. When the temperature changes, it causes changes in dielectric properties. Since capacitance is directly proportional to dielectric constant, the capacitance changes with temperature.

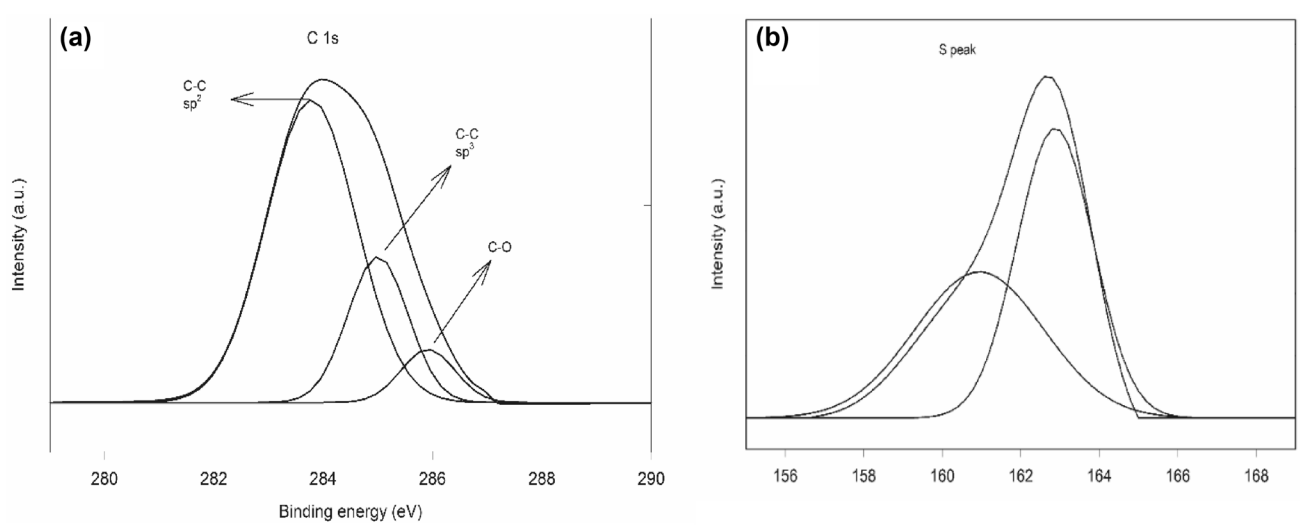

Fig. 2 XPS spectra of the prepared S-doped DLC nanocomposite

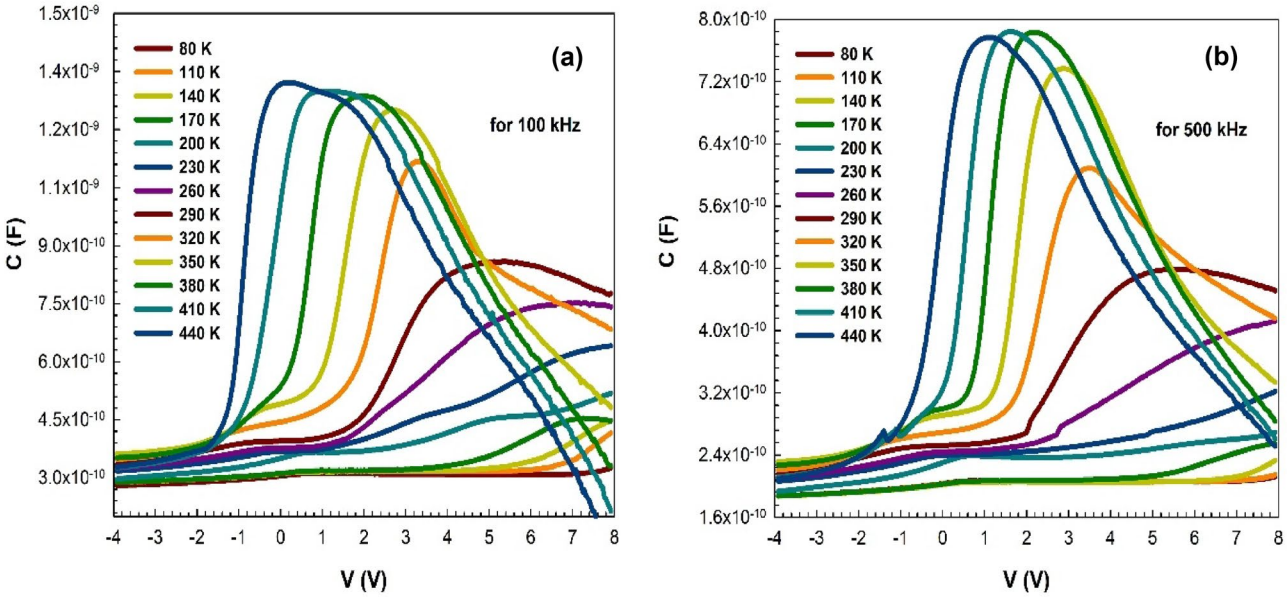

Fig. 3 *C–V–T* curves of the Au/(S-DLC)/p-Si device **a** 100 kHz and **b** 500 kHz

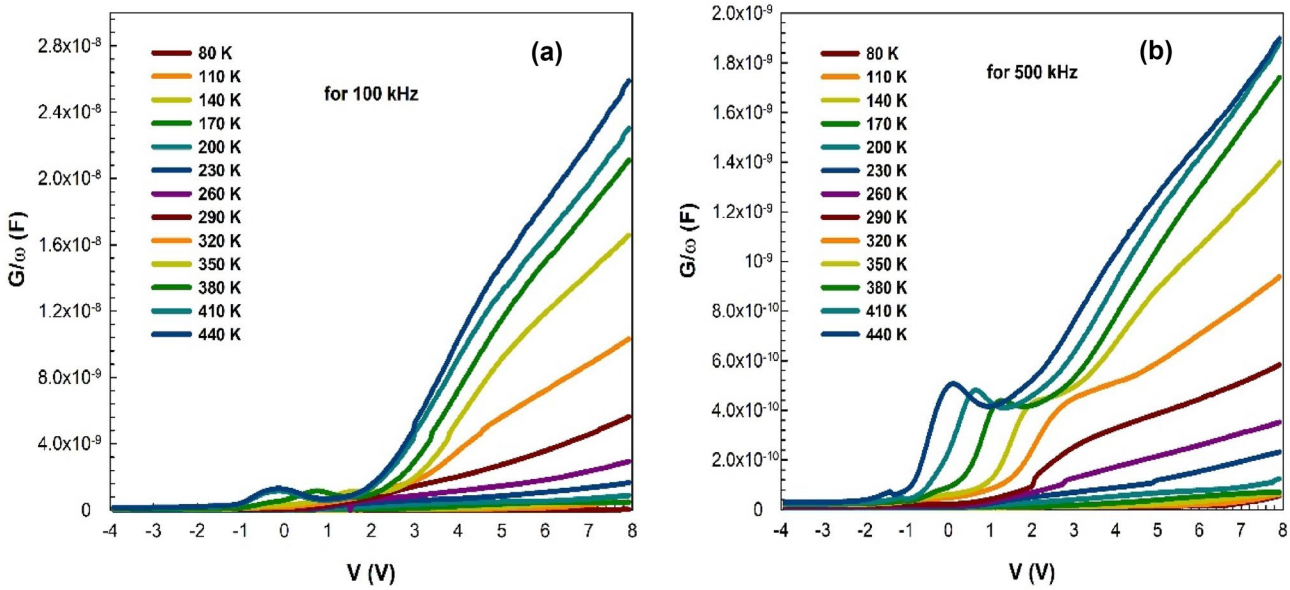

Fig. 4 *G/ω–V–T* curves of the Au/(S-DLC)/p-Si device **a** 0.1 MHz and **b** 0.5 MHz

The observed increase both in the C and G/ω with increasing temperature is the result of the excitation of many electronic charges from valence band or traps to the conductance band under temperature and external electric field effects [23–26]. It is well known that at absolute temperature and very low temperatures, almost all electrons are considered frozen and so they have not enough thermal energy to move from the valence band to conductance band or over the barrier height. However, very little conduction can only be achieved through traps located between the metal and the semiconductor and in the forbidden energy gap. When the temperature increases, many electrons gain sufficient thermal

energy to over to barrier height. As a result, the conduction will increase with the temperature and bias voltage.

As shown in Fig. 3a and b and Fig. 4a and b, both the value of the C and G/ω decreased as the frequency increased. This frequency dependence of C and G results from the frequency response of the interface states or traps (N_{ss}) depend on their lifetimes or relaxation times (τ) [20, 25–28]. At low frequencies, the period ($T = 1/2\pi f$) is higher than the τ of the N_{ss}. In this situation, they can easy follow the ac signal. Therefore, the C value is high at low frequencies. At higher frequencies, the opposite of this situation occurs. On the other hand, while N_{ss} may be dominated in inversion/depletion regimes at moderate frequencies, R_s of the device is particularly dominant only at the accumulation regime ($G = 1/R_s$) at enough high frequencies. Thus, the real value of R_s can be calculated from the strong accumulation zone using Nicollian–Brews method ($R_s = G/(G^2 + (\omega C)^2)$) [20]. Figure 4a and b shows the ($G/\omega - V$) curves as a function of voltage at different temperatures and for frequencies of 0.1 MHz and 0.5 MHz, respectively. As seen in these figures, the conductance increases with an increase in temperature due to the thermally activated conduction process. Because, more and more thermally generated electronic charges increase with increasing temperature. In addition, conductance with frequency exhibits similar behavior with capacitance.

Additionally, the temperature sensitivity ($S = dV/dT$) of the structure was analyzed using voltage–temperature (V–T)-dependent capacitance values. Figure 5a and b shows the variation of voltage with temperature (between 290 and 440 K) at different constant capacitance values for 100 kHz and 500 kHz, respectively. From Fig. 5a, the S values were found to be about -26 mV/K and – 28 mV/K for 6 nF and 7 nF, respectively. From Fig. 5b, the S values were found to be about – 21 mV/K and – 24 mV/K for 3 nF and 4 nF, respectively. The sensitivity value increases with increase in constant capacitance value. The obtained result is in agreement with similar studies in the literature [29–31]. It is clear that the structure demonstrates very high temperature sensitivity.

3.4 Dielectric properties

Using the dielectric spectroscopy method, the basic dielectric parameters and conductivity properties of a dielectric material can be measured depending on frequency, temperature, and applied bias voltage or electric field. The dielectric processes are usually depending on interlayer, its thickness and homogeneity, N_{ss} and their τ, frequency, temperature, and applied external electric field [32]. The interlayer material can be easily polarized because of the electrons at surface states and dipoles may be easily restructured

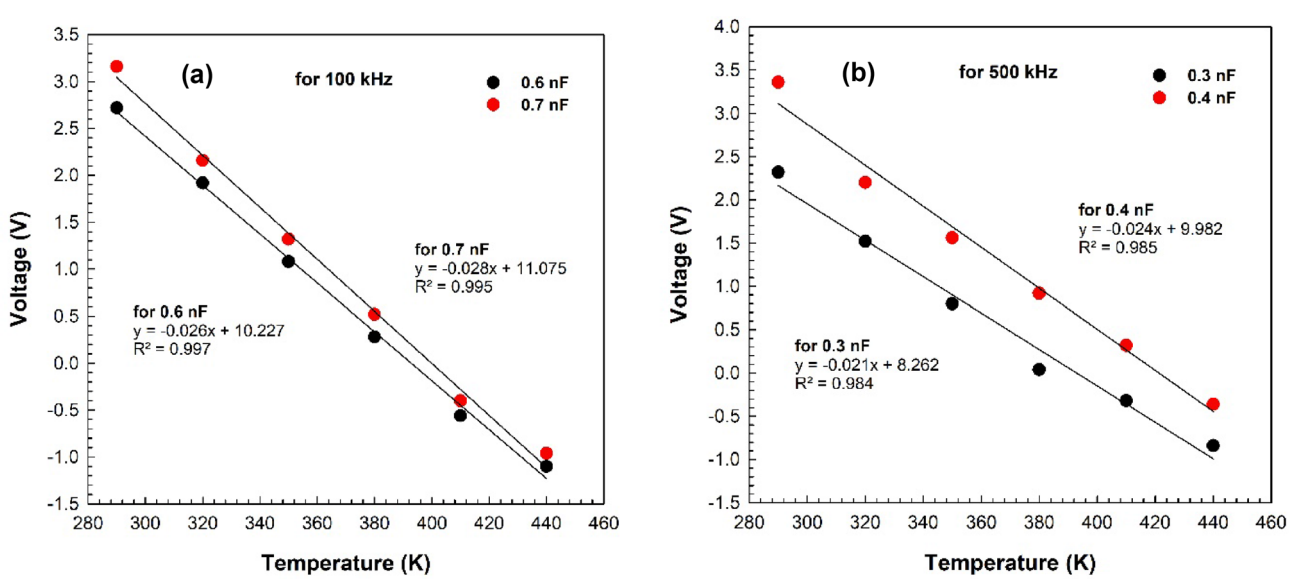

Fig. 5 **a** Applied voltage vs. temperature plots at different capacitance values for **a** 100 kHz and **b** 500 kHz

by reordering under electric field and temperature, especially at lower frequencies, but at higher frequencies, the dielectric value decreases due to shorter time available for the dipoles to align [33]. The observed decrease in ε' and ε" at high frequency is the result of a decrease in the polarization and also N_{ss} [6, 20]. In other words, the contribution of polarization and N_{ss} at lower frequency is quite higher than high frequencies [34–36].

A dielectric material has very low conductivity at dc voltage. The complex dielectric (ε*) including the real (ε') and imaginary (ε") parts is given as follows [37, 38]:

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \frac{C_m}{C_0} - j\frac{G_m}{\omega C_0}, \tag{1}$$

where Co is the capacitance of the empty capacitor and is given as follows [38]:

$$C_0 = \frac{\varepsilon_o A}{d}.$$

In Eqs. 1 and 2, the C_m and G_m are the measured C and G values, A is the Schottky contact area, and d is the interlayer thickness. While ε' is the measure of the energy stored in the polarized dielectric material, ε" is the loss energy. The magnitude of ε' and ε" is determined from Eq. 2. In addition, the dielectric loss tangent (tanδ) which is called as dissipation factor is defined as follows:

$$\tan(\delta) = \frac{\varepsilon''}{\varepsilon'} = \frac{1}{\omega RC}. \tag{3}$$

The temperature-dependent changes in ε', ε'', and tanδ values are given in Fig. 6a–c, respectively. As shown in these figures, while their values increase with increasing temperature, they decrease with increasing frequency. Since the temperature becomes increased, dipole orientations become easy and hence orientation polarization increases. This behavior causes an increase in dielectric constant [25, 39–45]. Besides, the observed increase in ε' value results from the contribution of the electronic charges to the polarization. In addition, the dielectric loss increases as the mobility of electronic charges increases with increase in temperature. As the frequency increases, ε' and ε'' value decrease due to polarization effects [46–49]. Especially, at low frequencies, space charge polarization or interfacial polarization is effective and hence, the magnitude of ε' becomes high at low frequency.

3.5 Electric modulus

Complex electric modulus ($M^* = M' + jM''$) is given as follows [41, 50–53]:

$$M^* = \frac{1}{\varepsilon^*} = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2}. \tag{4}$$

Figure 7a and b indicates a plot of M' and M'' as a function of temperature for two frequencies. As seen in these figures, while M' value decreases with increasing temperature, M'' value increases. Both M' and M'' values have an almost constant value below room temperature.

3.6 Electrical ac Conductivity

The AC electrical conductivity (σ_{ac}) is given as follows:

$$\sigma_{ac} = \varepsilon_0 \omega \varepsilon'' = \omega \varepsilon_0 \varepsilon' \tan\delta. \tag{5}$$

Figure 8 indicates the ac conductivity with temperature for two frequencies. As seen in this figure, the ac conductivity has an almost constant value below room temperature. Above room temperature, the ac conductivity increases rapidly by increasing temperature. Moreover, the value of σ_{ac} increases with the increasing frequency. The increase of σ_{ac} with temperature is due to the increase in thermally generated carriers [41, 53–56]. In other words, the increase of σ_{ac} results from the increasing drift mobility of electronic charges through hopping conduction.

As shown in Fig. 8, the value σ_{ac} increases with temperature and it was considerably high at enough high temperatures, but at low temperatures, it remains almost independent of temperature for both frequencies. Such behavior of it at high temperature is typical of semiconductor behavior. The conductivity is treated as temperature-activated hopping from center to center. There are many reports on the ac conductivity in the literature, to evaluate of activation energy (E_a) from the Arrhenius plot [41–43]:

In addition, the value of activation energy (E_a) of conductivity was estimated using the Arrhenius equation. Arrhenius equation is defined as follows [43, 57–61]:

$$\sigma_{ac(T)} = \sigma_0 \exp\left[\frac{-qE_a}{k_B T}\right], \tag{6}$$

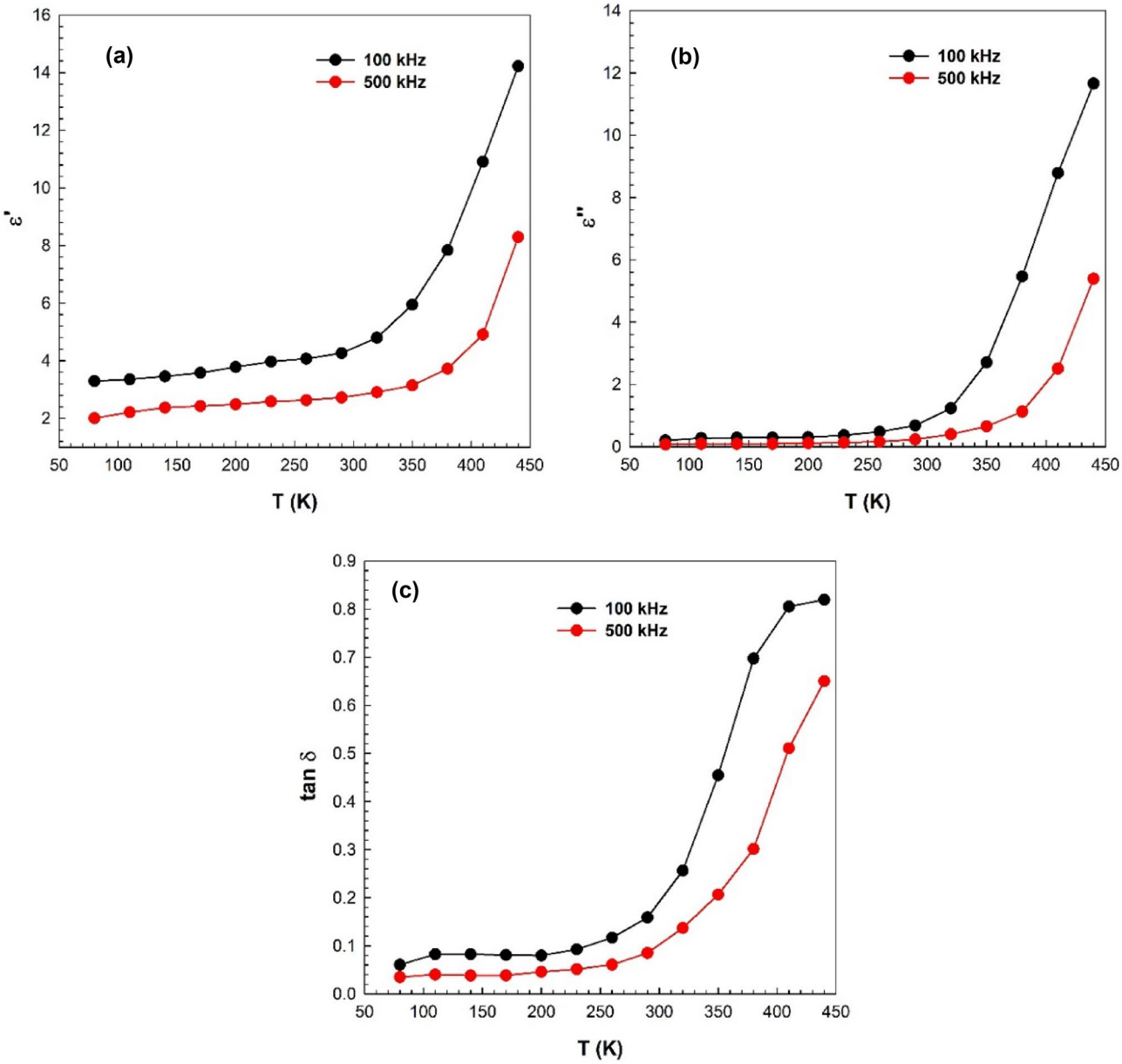

Fig. 6 **a** $\varepsilon' - T$, **b** $\varepsilon'' - T$, and (c) tan $\delta - T$ plots of the Au/(S-DLC)/p-Si device at 100 and 500 kHz, respectively

where σ_o is an exponential factor and k_B is the Boltzmann's constant. As shown in Fig. 9, the σ_{ac} vs T^{-1} plot has good straight line and the slope of this plot gives to us a direct E_a. It is clearly that the σ_{ac} vs T^{-1} plot has two distinctive linear part which are called as Region-1 (80–230 K, and Region-2 (260–440 K), respectively. Such behavior of it can be explained in terms of the hopping of electrons between interface traps. The calculated E_a and σ_0 values are given in Table 1. Both E_a and σ_0 values increase with increase in temperature. Also, while these values decrease with increasing frequency at lower temperatures and then increase at high temperatures.

All these results are indicated that the C, G/ω, and σ_{ac} values are very sensitive to temperature especially at and above room temperatures due to activated many electrons under temperature effect. This change in their values from voltage region to other or traps to traps is the result of thermal re-order/

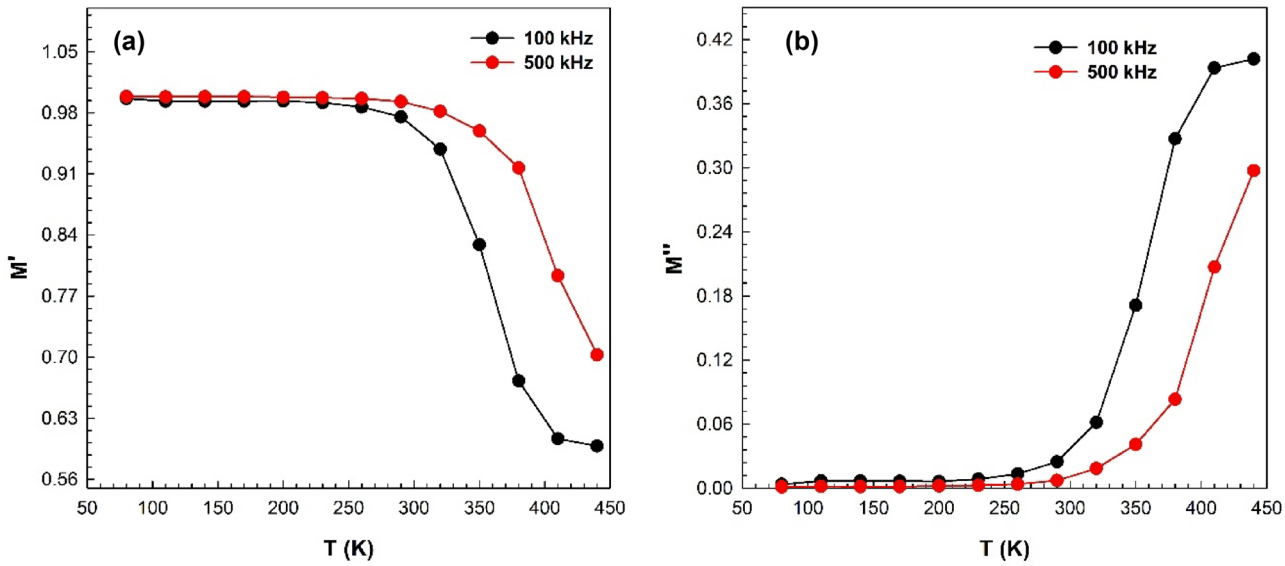

Fig. 7 **a** $M' - T$ *and* **b** $M'' - T$ plots of the Au/(S:DLC)/p-Si device at 100 and 500 kHz, respectively

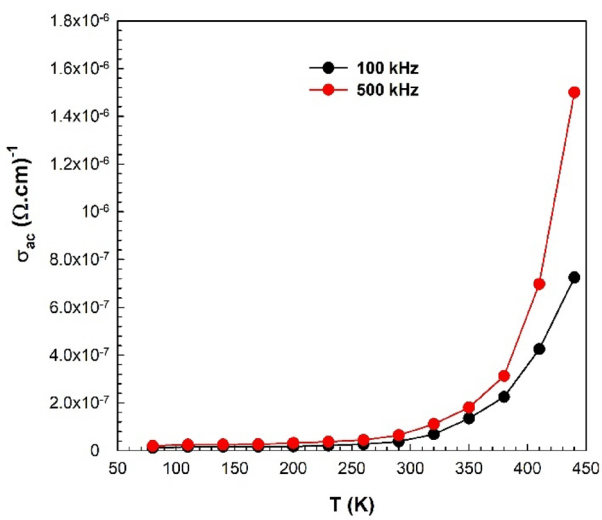

Fig. 8 Temperature-dependent σ_{ac} in the Au/(S:DLC)/p-Si device at 0.1 and 0.5 MHz

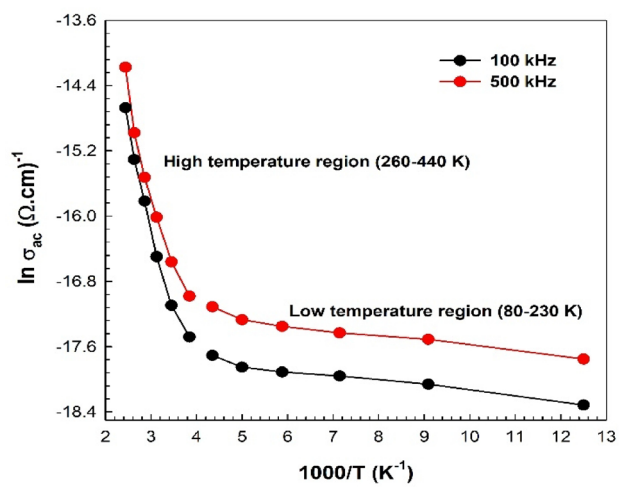

Fig. 9 Arrhenius plots of the Au/(S:DLC)/p-Si device at 100 and 500 kHz

Table 1 The calculated E_a and σ_0 values

Region-1 (80–230 K)			Region-2 (260–440 K)		
f (kHz)	E_a (meV)	σ_0 $(\Omega\ \mathrm{cm})^{-1}$	f (kHz)	E_a (meV)	σ_0 $(\Omega\ \mathrm{cm})^{-1}$
100	6.04	4.62×10^{-8}	100	186.56	7.56×10^{-5}
500	5.78	2.56×10^{-8}	500	189.41	1.35×10^{-4}

structure of the electronic charges under temperature and electric field effects.

4 Conclusion

In this study, (S:DLC) interfacial layer was sandwiched between metal (Au) and semiconductor (p-Si) using electrodeposition method using methanol as carbon source and thiophene as sulfur source. Firstly, the morphology

and chemical composition of the film were analyzed by SEM and XPS spectroscopy method. Secondly, the "Admittance or conduction technique" which is including a set of frequency or temperature-dependent C and G/ω measurements of performed Au/S-DLC/p-Si device both at 100 kHz and 500 kHz in the frequency range of 80–440 K and voltage range of (− 4 V)–8 V. After that the real (ε') and imaginary (ε'') components of the complex dielectric (ε^*) and (M') and (M'') of the complex electric modulus (M^*), tanδ, and ac conductivity (σ_{ac}) values were calculated from these C and G data. The values of ε', ε'', and σ_{ac} were usually increased with increasing temperature, but this change becomes more prominent especially at above room temperature. As the dielectric parameters decrease with increasing frequency, the ac conductivity increases. The E_a value of the Au/S-DLC/p-Si device was obtained from the slope of the straight line of the Arrhenius plot (ln(σ_{ac} − 1000/T) for 100 kHz and 500 kHz. The observed two linear parts of Arrhenius plot show that there is two different conduction mechanisms at low and high temperatures, respectively. The observed higher values of E_a and ε' (~ 14) even at 100 kHz indicated that hopping of electrons between traps is effective charge transport mechanism and so the prepared Au/(S:DLC)/p-Si/Au structure can be used to store more energy and temperature sensor.

Author contributions

The manuscript was written with the contributions of all authors. All authors have approved the final version of the manuscript. AT contributed to investigation, data curing, and writing, reviewing, and editing of the manuscript. HD contributed to investigation, measurements, and reviewing and editing of the manuscript. AFV contributed to sample preparation, measurements, and reviewing and editing of the manuscript. BA contributed to sample preparation, measurements, review and editing of the manuscript, and supervision. SA contributed to investigation, writing, reviewing, and editing of the manuscript, and supervision.

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Data availability

The datasets analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest There are no conflicts to declare.

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