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Topology-Morphing Photovoltaic Microconverter with Wide MPPT Voltage Window and Post-Fault Operation Capability

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ABSTRACT In this paper the concept of wide input voltage range photovoltaic microconverter with post-fault operation capability is presented. This microconverter could remain operational in the case of short- or open-circuit failure of any switch of its front-end inverter. When the fault occurs, the control system automatically identifies the fault and applies the special post-fault modulation sequence thus keeping the functionality of the microconverter unchanged. The research findings are validated by the help of a 350 W experimental prototype specially developed for integration of silicon PV modules into the residential DC nanogrids with the nominal voltage of 350 V. Paper explains the multi-mode operation principle and fault identification routine. It presents the experimental efficiencies and evaluates the maximum power point tracking performance of the microconverter prior and after the short-circuit fault of an upper switch of the inverter. The daily energy yield test conducted for both cases has confirmed that the proposed approach can extend the service life of PV microconverters with a moderate impact on their performance.

INDEX TERMS DC-DC power converters, digital control, fault diagnosis, fault tolerance, fault-tolerant control, photovoltaic systems, power electronics, pulse width modulation, quasi-Z-source converters.

I. INTRODUCTION

In residential and small commercial photovoltaic (PV) installations the application of module-level power electronics (MLPE) systems typically allows for better mitigation of power losses caused by various partial shading effects as well as mismatch and aging of PV modules [1]-[3]. The industrial MLPE systems today are broadly represented by the power optimizers and microinverters, which are the weather-proof devices usually located outdoors just behind the PV module or embedded in its frame [4]. Oppositely to power optimizers, which foresee a series connection of PV modules, the use of a microinverter offers a possibility of direct integration of PV modules to the AC grid. Having the multistage structure, the microinverter tracks the maximum power point (MPP), steps up and inverts the output voltage of the PV module into a grid compliant AC voltage. In the last decade with the appearance of the emerging concept of the household DC distribution [5] the group of MLPE systems was expanded by the microconverters, which are used for DC integration of the PV modules [6]. In contrast to power optimizers, the microinverters and microconverters typically have a more narrow input voltage regulation range, which significantly limits their shade-tolerant performance and compatibility with different types of PV modules. However, this issue was recently addressed by the implementation of advanced topology-morphing and multi-mode control principles [7]-[9], which resulted in the appearance of a novel class of the hybrid MLPE systems called Optiverter [10].

In general, being mounted just behind the PV module the MLPE devices are subjected to a harsh operating conditions.

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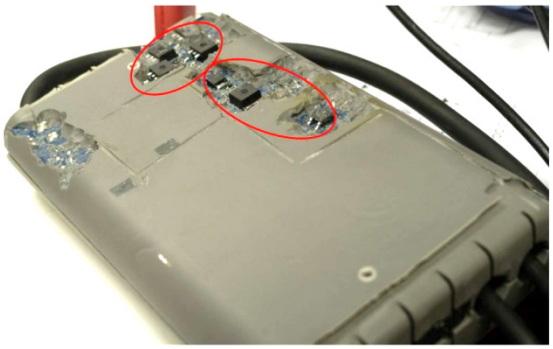


FIGURE 1. Photo of the disassembled PV microinverter with the thermally conducting epoxy removed at the locations of possible faults.

This includes wide variation in temperatures, excess humidity, vibrations, dust and snow deposition, etc. [11]. For example, in several hot or high irradiance locations, the ambient temperature of the MLPE system could reach or ever exceed 50 ^{0}C thus elevating the internal temperature stress of the device over 75 ^{0}C. Moreover, the enclosure of MLPE device should have a high IP-rating to withstand different weather conditions like rain and wind. It has to protect the electronics from the aggressive environment within the expected lifetime, which typically exceeds 20 years [12]. For that purpose, the majority of MLPE devices are filled with a water-resistant thermal epoxy to "pot" the components and move the heat away from the hotspots to the enclosure, at the same time providing the humidity-resistant protective layer. This ensures a necessary IP rating and thermal management for the cost of maintainability as the malfunctioned or damaged potted device is unlikely to be easily repaired (Fig. 1). Typically, the faulty MLPE device is replaced with a new one according to the terms and conditions of the sales warranty or servicing contract. However, the clarification of warranty issues could be a time-consuming process resulting in the increased potential economic loss due to the downtime of the PV power system.

This paper studies the post-fault operating capability of a high-performance PV microconverter in the case of power switch failure in its front-end inverter. The topology-morphing control (TMC) is proposed as a tool for ensuring the necessary level of self-redundancy without adding extra elements to the circuit. The paper starts with the general description of the proposed microconverter and its specifications. Next, the basics of TMC and multi-mode operation principle of the microconverter are explained in Section 3. Section 4 describes the algorithm for the fast detection of the faulty switch in a front-end inverter. The experimental study in Section 5 demonstrates the performance of the proposed microconverter in the normal and post-fault operation, which is followed by the conclusions drawn in Section 6.

II. FAULT-TOLERANT PV MICROCONVERTER

The idea proposed in this paper was inspired by a high-performance multi-mode series resonant PV microconverter presented in [8]. This baseline microconverter was intended for operation within an ultrawide input voltage and load range (i.e., from 10 to 60 V and from 30 to 300 W), which provided an opportunity of realization of a Global MPPT (GMPPT) based on a periodic P-V curve sweep [13]. Moreover, the ultra-wide input voltage range enabled the unique multi-module compatibility feature, which allows this microconverter to be paired with many existing PV module technologies ranging from the classic 60- and 72-cell Si panels [14] to the advanced PV roofing elements [15]. In this study, the performance of a concept from [8] is further enhanced by adding a possibility of post-fault operation, which guarantees the supply continuity in the case of failure of any of the front-end inverter switches.

A. TOPOLOGY AND SPECIFICATIONS

The generalized power circuit diagram of the fault-tolerant microconverter (FT-MIC) is shown in Fig. 2*a*. Its general view and operating power envelope are shown in Fig. 3. At the input side, the FT-MIC has an active quasi-Z-Source Network (qZSN) coupled with the Hybrid Switching Cell (HSC). This part performs the MPPT and generates the high-frequency AC voltage for supplying the step-up isolation transformer *TX*. The reconfigurable rectifier (RR) implemented at the output side of the FT-MIC is used for compensation of the voltage gain reduction in the post-fault operation mode.

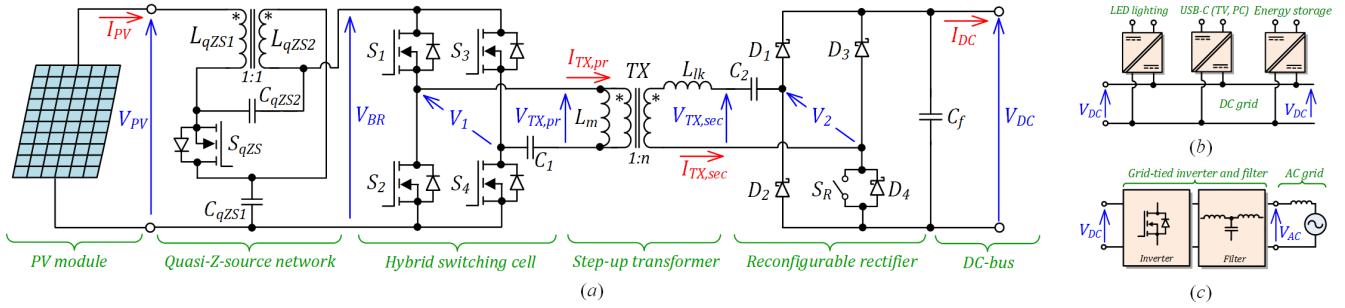


FIGURE 2. Generalized topology of the proposed fault-tolerant PV microconverter (*a*) and its application possibilities in the household DC nanogrid (*b*) or as a front-end of the two-stage grid-tied PV microinverter (*c*).

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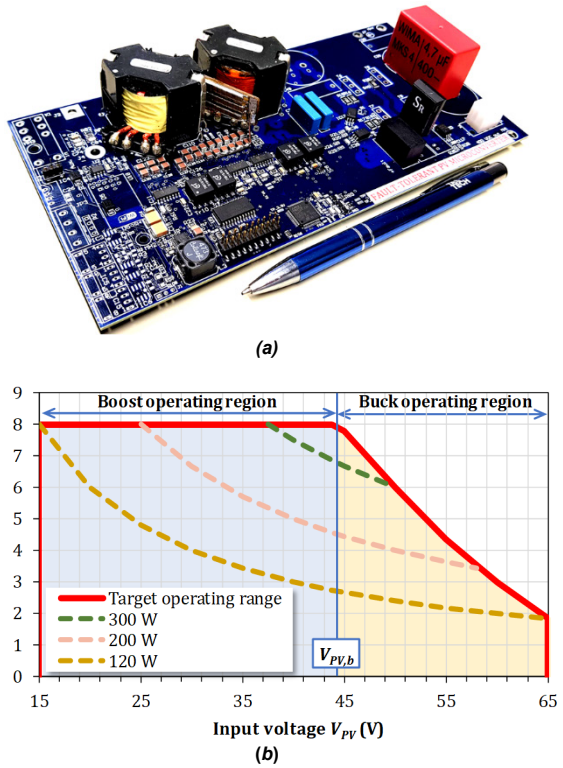
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Although this microconverter is primarily designed for feeding the PV power into the household DC nanogrid (Fig. 2*b*), which could also be used as a front-end of the two-stage grid-tied PV microinverters (Fig. 2*c*).

The general specifications of the FT-MIC are listed in Table I. It was developed for the integration of 72- and 96-cell silicone PV modules into the residential DC nanogrids with the nominal voltage $V_{DC} = 350$ V. The proposed approach could be also adopted for other types of PV modules and output voltages by changing the turns ratio of the isolation transformer *TX*. The primary side of the FT-MIC employs HSC realized on the generic Si MOSFETs. As the qZSN usually requires two magnetic elements, which would impose weight and power density constrains, the two-winding coupled inductor was implemented thus leading to a more compact and lightweight design. To improve the performance and enable the multi-mode control of the FT-MIC, the diode of the qZSN was replaced by the Si MOSFET. The output side of the microconverter is realized on SiC Schottky Barrier Diodes in combination with the mode-changing switch/relay S_R, which is used for changing the topology and resulting voltage gain of the rectifier by shorting the diode D_4. The discussed FT-MIC is essentially a series-resonant isolated buck-boost converter that uses the hybridization of properties for enabling the ultra-wide input voltage without significant deterioration of the efficiency. In the boost mode, it operates as a hybrid of the quasi-Z-source and series resonant DC-DC converter (SRC), while in the buck mode, it resembles the SRC controlled by the phase-shift modulation (PSM). The series resonant tank is formed by the leakage inductance of the isolation transformer L_{lk} and capacitor C_2 utilized in the RR. As the quality factor of such an integrated resonant tank is significantly lower than unity the PSM control approach with discontinuous resonant current (DcPSM) was implemented thus allowing for the balanced cost-performance tradeoff that is important for the industrial design.

TABLE I
SPECIFICATIONS OF THE PROPOSED FT-MIC

Operating parameters	
Input voltage range, V_{PV}	15…65 V
Maximum input current, I_{PV}	8 A
Rated output voltage, V_{DC}	350 V
Switching frequency, f_{SW}	95 kHz
Dead-time of inverter switches	50 ns
Operating power range, P	35…350 W
Components	
Microcontroller	ST STM32F334R8T6 (CortexM4,72MHz)
S_1...S_4, S_{qZS}	ON Semiconductor / Fairchild FDMS86180
D_1…D_4	Wolfspeed C3D02060E
S_R	Single-pole normally open relay IXYS CPC1968
L_{lkqZS}	0.6 µH
L_{mqZS}	12 µH
L_{lk}	64 µH
L_m	1 mH
n	8
C_{qZS1}, C_{qZS2}	MLCC 26.4 µF (12 parallel KEMET C1210C225K1R)
C_1	MLCC 26.4 µF (12 parallel KEMET C1210C225K1R)
C_2	Metallized Polypropylene 66 nF (2 parallel EPCOS B32672Z6333K)
C_f	Metalized Polyester 4.7 µF WIMA MKS4G044706G



(*a*)

(*b*)

FIGURE 3. General view of the proposed FT-MIC (*a*) and its operating power envelope with predefined boost and buck regions and constant power operation limits (*b*).

B. HYBRID SWITCHING CELL

The idea of the HSC originates from [16], where it was proposed as an alternative realization approach of the bidirectional SRC with a possibility of post-fault operation in the case of short-circuit failure (SCF) or open circuit failure (OCF) of any of its semiconductors. The HSC shown in Fig. 4*a* has the full-bridge structure (S_1…S_4 in Fig. 2*a*), and in the case of a semiconductor switch failure, can be reconfigured to the asymmetric half-bridge by merely modifying the modulation sequence of its switches [17]. Such an idea of inherent fault tolerance considers that the damaged switch could be further used either as a conducting (SCF) or a non-conducting (OCF) circuit branch. Moreover, the opposite healthy switch in the same leg must be continuously turned off or on, thus realizing the post-fault reconfiguration of the HSC in the case of SCF or OCF, correspondingly. As the post-fault modulation sequences of

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the HSC are identical for both fault types and different fault locations, the SCF of S_1 will be used as a case study in the remainder of this paper.

As it was previously mentioned, in the case of SCF of S_1, the opposite switch S_2 in the same leg must be continuously turned off to avoid the short-circuit of the input voltage source (Fig. 4*b*). As the damaged switch creates the current-conducting circuit path, one of the AC terminals of the RR becomes connected to the DC rail of the HSC. The switches S_3 and S_4 of the healthy leg are controlled complementary and generate the unipolar pulsed voltage V_1. For making the output AC voltage $V_{TX,pr}$ bipolar, the HSC employs the DC blocking capacitor C_1 which could also perform a function of the resonant capacitor [18].

In a similar way, the reconfiguration approach is applied to the quasi-Z-source galvanically isolated DC-DC converters (qZSC), where in the case of SCF of the switch S_1, the HSC could be reconfigured into a single-switch qZSC (Fig. 4*c*). In that case, the switch S_2 is continuously turned off to avoid the short-circuiting of the impedance-source network. The switch S_4 is permanently turned on thus connecting the DC rail of the HSC to its output AC terminal. The voltage gain is controlled by the duty cycle D of the switch S_3. During the off-state of the S_3, the transformer TX is supplied from the qZSN with the unipolar voltage pulses, and the capacitor C_1 acts as the DC blocking capacitor that prevents the transformer core from the saturation [19].

C. RECONFIGURABLE RECTIFIER

After the described post-fault reconfiguration of the HSC into a half-bridge or single-switch topology, the resulting DC voltage gain of the microconverter is reduced twofold. To keep the output voltage unchanged the FT-MIC features the reconfigurable rectifier (RR) which can compensate the gain reduction by the reconfiguration from a full-bridge to a Greinacher voltage-doubler structure (Fig. 5). For that purpose the mode-changing switch/relay S_R is turned on, thus connecting one of the AC terminals of the RR to the output of the microconverter. The opposite diode in the same leg (D_3 in Fig. 5*b*) becomes reverse-biased, and the rectification is done only by the diodes D_1 and D_2. Such shorting of a diode in a full-bridge rectifier offers the simplest way of the topology morphing and requires a single relay with the corresponding control circuitry. For more demanding applications, the use of a semi-controlled RR could be also considered, which can offer slightly better efficiency for the cost of a more complex realization and control [20]. Moreover, in the case of a full-controlled RR the microconverter could be kept operational even at a simultaneous failure of one of the switches in its primary and secondary sides [16].

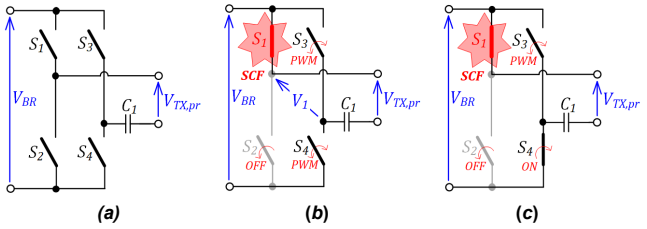


FIGURE 4. Hybrid switching cell (*a*) with examples of its reconfiguration in the case of SCF of the switch S_1: asymmetric half-bridge (*b*) and single-switch ISC (*c*).

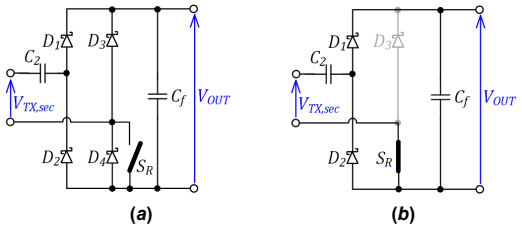


FIGURE 5. Reconfigurable rectifier (*a*) with an example of its reconfiguration into the Greinacher voltage-doubler topology by shorting the diode D_4 (*b*).

D. MULTI-MODE CONTROL

One of the key features of the proposed FT-MIC is that it can remain operational after the SCF of OCF of any switch of the HSC. Moreover, after the fault, the microconverter can still ensure the wide DC gain range similar to the normal operation. For enabling that, the buck-boost multi-mode control was applied in both cases (Fig. 3*b*). Thanks to unique control flexibility offered by the qZSC [21], the buck-boost functionality was realized in a single switching stage, i.e., in the HSC. Next, the operation and control principle of the FT-MIC during the normal and post-fault operating conditions are described in detail.

III. NORMAL OPERATION

Throughout its prognosed lifetime, the proposed FT-MIC will operate as a full-bridge quasi-Z-source SRC with the full-bridge rectifier (Fig. 2*a*). Similarly to the baseline topology [8], the input voltage regulation range is divided into two regions – boost and buck operation regions - with the boundary point $V_{PV,b}$, which is used for selection of the turns ratio n of the step-up isolation transformer (Fig. 3*b*):

$$n = \frac{V_{DC}}{V_{PV,b}}. \tag{1}$$

As the $V_{PV,b}$ in the given case study was set to 44 V, the isolation transformer with the turns ratio $n = 8$ was selected for ensuring the demanded DC voltage gain.

When the operating point of the FT-MIC moves to the boost region ($V_{PV,boost} = 15\ldots44$ V, see Fig. 3*b*) it starts operation as a full-bridge quasi-Z-source SRC controlled by the shoot-through PWM (ST-PWM) at the resonant frequency. The DC voltage gain is regulated by the variation of the shoot-through duty cycle:

$$G_{N,boost} = \frac{V_{DC}}{nV_{PV}} = \frac{1}{1-2D_{ST}}, \tag{2}$$

where D_{ST} is the cumulative duty cycle of the shoot-through

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states over the switching period T ($D_{ST} = t_{st}/T$). The shoot-through states are generated by the cross-conduction of all switches of the HSC that occur twice per switching period.

If the operating point is located in the range from 44 V to 65 V (Fig. 3*b*), the microconverter starts operation in the buck mode, and the DcPSM regulates the output voltage at the resonant frequency. The application of this control method to the impedance-source galvanically isolated DC-DC converters was described in [22]. In the DcPSM, the switch S_{qZS} is always conducting which bypasses the qZSN, and the microconverter operates similarly to the classical voltage-source SRC. The output voltage is controlled by the phase shift angle φ between the leading (S_1 and S_2) and lagging (S_3 and S_4) legs of the HSC. The control characteristic of the FT-MIC in the buck mode depends strictly on the quality factor Q of the resonant network:

$$G_{N,buck} = \frac{V_{DC}}{nV_{PV}} = 0.5\left[A\left(\frac{2}{\pi Q} - 1\right) + \sqrt{\left(\frac{2}{\pi Q} - 1\right)^2 A^2 + A\frac{8}{\pi Q}}\right], \quad (3)$$

where

$$A = 0.5 - 0.5 \cdot \cos\left[\pi \cdot \left(1 - \frac{\phi}{180}\right)\right] \text{ and } Q = \frac{8\pi f_{SW} L_{lk}}{R_L}. \quad (4)$$

Fig. 6 shows the experimental control variables of the FT-MIC for the normal operation at different power levels considering the limitations shown in Fig. 3*a*. In the ST-PWM boost region, the FT-MIC has linear control characteristics with almost no dependence on the operating power. However, in the PSM buck region, the FT-MIC gain (4) strictly depends on the load R_L that is proportional to the Q-factor of the integrated series resonant tank.

The experimental operating waveforms of the FT-MIC during the normal operation at 300 W are shown in Fig. 7. Assuming $C_1 \gg n \cdot C_2$, the leakage inductance of the isolation transformer resonates only with the capacitor C_2, which ensures zero-current switching of the rectifier diodes. At the same time, the transformer magnetizing current provides the soft-switching of HSC transistors at any load. The voltage swing across the resonant capacitor C_2 equals 68 V, which is in a good agreement with (5).

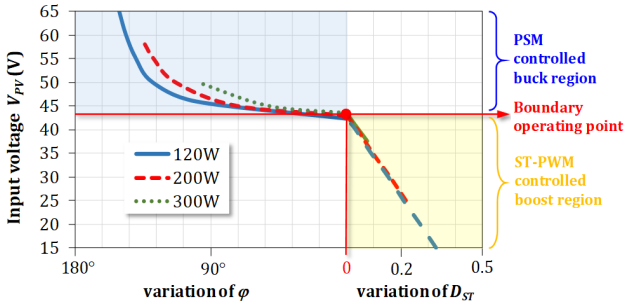


FIGURE 6. Normal operation of the proposed PV-MIC: operating regions, modulation methods and experimental control variables at different constant operating power levels.

$$\Delta v_{C2(N)} = \frac{P}{2 \cdot f_{SW} \cdot V_{DC} \cdot C_2}. \quad (5)$$

During normal operation, the FT-MIC features a full symmetry of operation thus the average voltages of C_1 and C_2 remain zero within the whole operating range.

IV. RECONFIGURATION AND POST-FAULT OPERATION

In the case of SCF of an HSC switch, the FT-MIC is reconfigured either into a single-switch qZSC or an asymmetric half-bridge converter. The topology morphing scenario depends on the operating point and is realized by applying one of the post-fault modulation sequences. The reduction of a voltage gain after the reconfiguration is compensated by the activation of the switch/relay S_R, which changes the structure of RR to a Greinaher voltage doubler rectifier (GVDR). Next, the case study scenario of the post-fault operation after the SCF of a switch S_1 is discussed.

In the boost region, i.e., from 15 V to 44 V, the reconfigured FT-MIC starts operating as a single-switch qZSC with GVDR [23]. The post-fault modulation sequences of the FT-MIC in the boost region are presented in Table II for different faults. The selected fault scenario is visualized in Fig. 8*a*. The DC voltage gain is regulated by the variation of a common duty cycle D of the diagonal pair of healthy switches (S_2 and S_3 in the case of SCF of S_1) controlled synchronously:

$$G_{PF,boost} = \frac{V_{DC}}{nV_{PV}} = \frac{1}{1-2D}. \quad (6)$$

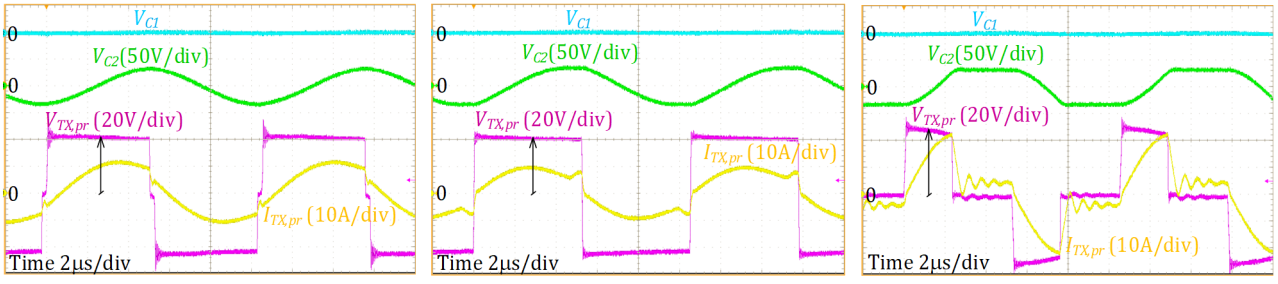


FIGURE 7. Experimental waveforms of the proposed FT-MIC during the normal operation at 300 W in three different operating points: in a boost region at V_{PV} = 40 V and D_S=0.046 (*a*), boundary operating point $V_{PV,b}$ = 44 V (*b*) and in a buck region at V_{PV} = 50 V and φ =100⁰ (*c*).

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The switch S_{qZS} conducts current only during the off-state of S_2 and S_3. To avoid cross-conduction of the diagonal switches and S_{qZS}, the dead-time should be added between their switching transients. During the off-state of the switches S_2 and S_3, the primary winding of the transformer *TX* is supplied from the qZSN with the unipolar voltage pulses through the capacitor C_1 that acts as the DC-blocking capacitor preventing the transformer core from saturation.

In the buck region, i.e., from 44 V to 65 V, the topology of HSC is reconfigured to the asymmetric half-bridge, while the switch S_{qZS} is turned on permanently (Fig. 8*b*). The other switch in the leg with the SCF is turned off continuously to avoid the short circuit of the input side. The transistors in a healthy leg of the HSC are being switched alternately with a deadtime. One of these switches is conducting for a time interval shorter than half of the switching period, i.e., its duty cycle is always smaller than 0.5. The duty cycle of the opposite switch becomes larger than 0.5, which results in the asymmetrical voltage V_1 at the output terminals of the inverter bridge. The capacitor C_1 of the HSC is used as a DC-blocking cap to avoid the saturation of the transformer magnetic core. The resulting difference in duty cycles ΔD_a is used as a control variable in the buck region. The post-fault modulation sequences for different fault scenarios of the FT-MIC operating in the buck region are presented in Table III and the selected case study with SCF of S_1 is visualized in Fig. 8*b*. It should be noted that the qZSN in the post-fault buck mode is permanently bypassed by keeping the S_{qZS} continuously conducting. This helps to avoid the influence of the qZSN on the output voltage regulation [24] so the DC gain of the FT-MIC could be controlled similarly to that of the voltage-source series resonant converters [25], [26]:

TABLE II
POST-FAULT MODULATION SEQUENCES IN THE BOOST REGION

Faulty device	S_1	S_2	S_3	S_4	S_{qZS}	S_R
S_1	**SCF**	PWM	PWM	ON	$\overline{\text{PWM}}$	ON
S_2	PWM	**SCF**	ON	PWM		
S_3	PWM	ON	**SCF**	PWM		
S_4	ON	PWM	PWM	**SCF**		

TABLE III
POST-FAULT MODULATION SEQUENCE IN THE BUCK REGION

Faulty device	S_1	S_2	S_3	S_4	S_{qZS}	S_R
S_1	**SCF**	OFF	PWM	$\overline{\text{PWM}}$	ON	ON
S_2	OFF	**SCF**	PWM	$\overline{\text{PWM}}$		
S_3	PWM	$\overline{\text{PWM}}$	**SCF**	OFF		
S_4	PWM	$\overline{\text{PWM}}$	OFF	**SCF**		

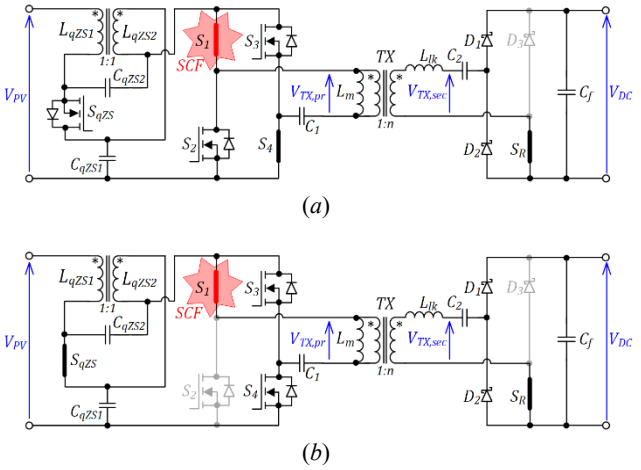


FIGURE 8. Power circuit of the proposed PV-MIC after the reconfiguration in the case of CSF of S_1: single-switch qZSC with GVDR in the boost region (*a*), and asymmetric half-bridge with GVDR in the buck region (*b*).

$$G_{PF,buck} = \frac{V_{DC}}{nV_{PV}} = \frac{1}{2}\left(\left(\frac{1}{2} - B\right)C + \sqrt{\left(B - \frac{1}{2}\right)^2 C^2 + 4BC}\right), \quad (7)$$

where

$$B = C_2 R_L f_{SW} \text{ and } C = 1 - \cos\left(\frac{\omega_r (1 - \Delta D_a)}{f_{SW}}\right). \quad (8)$$

Fig. 9*a* shows the experimental control variables of the microconverter for the post-fault operation at different power levels and considering the limitations from Fig. 3*a*. Similar to the normal operation, the FT-MIC features the resonant properties in the post-fault buck region, and its control characteristics depend strictly on the load conditions. In the boost region, the FT-MIC is capable of operating with the duty cycles starting from 0.12, which is imposed by the thermal limitations of passive convection cooling. The boost region can be extended to overlap with the buck region. This allows for the implementation of transition between the modes, as shown in Fig. 9*b*. A narrow voltage hysteresis band ensures stable operation during mode transition transients caused by the recharging of capacitors. The hysteresis transition between the microconverter modes is possible as all control variables can be pre-calculated for this.

The experimental operating waveforms of the microinverter during the post-fault operation at 300 W are shown in Fig. 10. The operation asymmetry is clearly seen in both the boost (Fig. 10*a*) and buck (Fig. 10*b*) operation points. Operating voltages of capacitors C_1 and C_2 have the DC component, which can be calculated from equations in Table IV. The voltage swing across the resonant capacitor C_2 is close to 140 V, which is in a good agreement with (9).

$$\Delta v_{C2(PF)} = \frac{P}{f_{SW} \cdot V_{DC} \cdot C_2}. \quad (9)$$

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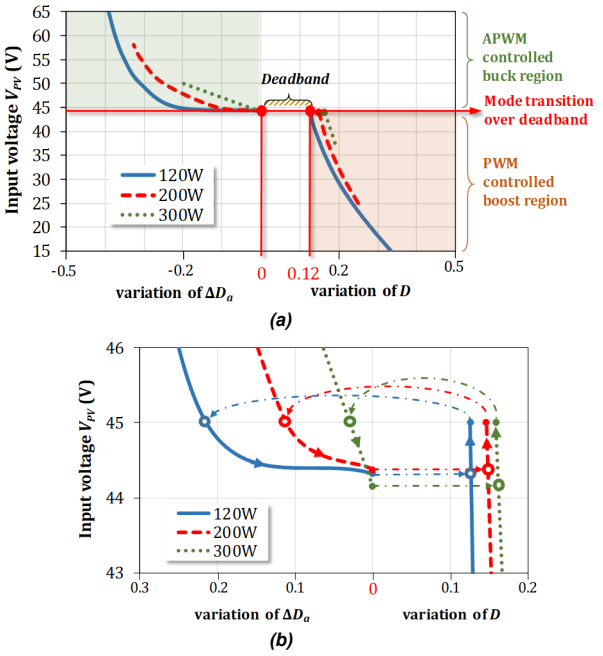


FIGURE 9. Post-fault operation of the proposed FT-MIC: operating regions, modulation methods, and experimental control variables at different constant power levels *(a)*, and hysteresis implementation of the transition between modes *(b)*.

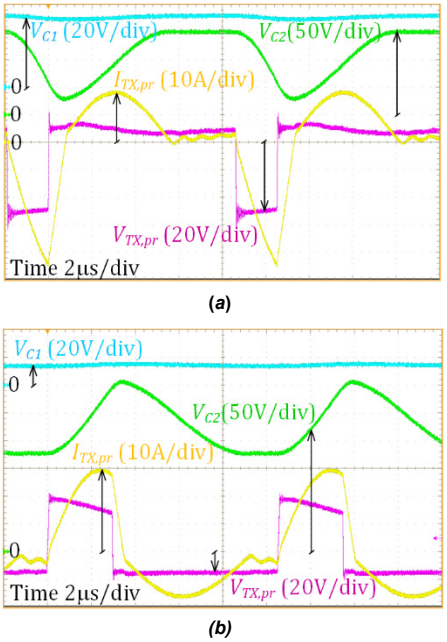


FIGURE 10. Experimental waveforms of the proposed FT-MIC during the post-fault operation at 300 W in the boost region at V_{PV} = 40 V and D = 0.18 *(a)* and in the buck region at V_{PV} = 50 V and ΔD_a = 0.2 (*b*).

TABLE IV
AVERAGE VOLTAGES OF C_1 AND C_2 AFTER RECONFIGURATION.

	Boost region	***Buck region***
C_1	$\frac{V_{PV}\cdot(1-D)}{1-2\cdot D}$	$V_{PV}\cdot(0.5-\Delta D_a)$
C_2	$\frac{V_{PV}\cdot n\cdot D}{1-2\cdot D}$	$V_{PV}\cdot n\cdot(G-0.5+\Delta D_a)$

V. FAULT IDENTIFICATION ROUTINE

There are several approaches to detect transistor faults during the converter operation. In high power circuits, where the cost of sensors is negligible compared to the cost of switches, additional measurement circuits could be used to detect the fault. In mid- and low-power circuits use of driver with fault detection feature might be used. However, the commercial drivers for MOSFETs have limited fault detection functionality. They are designed for SCF detection and, consequently, protect conventional voltage-source converters from failures in DC-link capacitors or remaining healthy switches [27]. Hence, additional measures are required for detecting the OCFs [28]. There are several methods capable of detecting both OCF and SCF at the cost of auxiliary sensors and digital signal processing: voltage sensing of magnetic components through auxiliary windings [29], diode voltage sensing [30], capacitor current sensing [31], inductor current sensing using custom Rogowski coil [32] or conventional sensors [33], etc. Their sensitivity and robustness to noise can be improved by employing artificial neural networks [34] or state observers [35], [36].

Another approach is to measure converter voltages and currents in the key points and compare them with a predefined pattern to detect a fault. This methodology is cheaper, but it has drawbacks – slow detection time and necessity to calculate patterns and values to be compared for each topology state separately. Still, this paper describes a fault detection method for the qZSC based on a measurement of a drain-source voltage across the bottom switches S_2 and S_4. In addition, the input voltage and current measurements, which are used for the MPP tracking, can be also used as input signals for the fault identification routine. Relatively slow fault identification time of the microcontroller unit (MCU) is a minor drawback due to the low sensitivity of a qZSC to abnormal conditions caused by the faults.

The proposed fault identification approach is based on the detection patterns that are compared to the measured values during operation. Table V presents reference voltages across the switches S_2 and S_4 during switching states of the converter in the normal operation. It is worth mentioning that the difference between these voltages equals the transformer voltage $V_{TX,pr}$ in the normal operation. Table VI shows six SCF cases out of many possible in the converter. Fault 1 describes SCF of one top transistor in the bridge. Execution of the fault detection routine by the MCU is described in Fig. 11. After the fault 1 occurs, the energy can still be transferred to the load during the first half-period, like in the normal operation. However, in the second half-period, the fault could be detected due to abnormal switch voltage V_{S4} according to Fig. 11. In this state, the microconverter could be reconfigured as proposed in Fig. 8. The fault 2 describes SCF of one bottom transistor, fault 5 – SCF of a top and a bottom transistor in different bridge legs. Reconfiguration for the fault 2 would be similar to that for the fault 1. The fault 5

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is one of the few cases of dual fault in semiconductors that can still be reconfigured to rover the converter, but only in the boost mode as this fault pattern is compatible with Fig. 8*a*. Dual-switch faults 3, 4, 6 listed in Table VI are not reconfigurable and result in permanent damage of the microconverter. However, the faults 4 and 6 allow for safe shutdown of the microconverter. The identification of OCFs is not described for brevity but can be implemented in the same way as the identification of SCFs.

Table VII shows the MCU parameters related to the fault detection routine. The analog to digital converter (ADC) embedded in the MCU was used for measurement of the voltages V_{S2} and V_{S4} synchronously with the PWM generation. The delays and trigger points used in this study are described in Fig. 11. High-resolution timer peripheral generates PWM signals and triggers ADC measurement. The ADC routines took 61% of MCU calculation time on average. However, the fault detection implemented with hardware abstraction layer (HAL) drivers could be optimized by employing low-layer library functions. In addition, a more powerful MCU with higher clock frequency could be used to decrease detection time when needed.

In order to test fault detection and evaluate fault tolerance, transistor S_2 was short-circuited randomly. The experiment was repeated several times. The worst-case among the measured SCF fault events is presented in Fig. 12. The blue and purple waveforms correspond to the voltages V_{S2} and V_{S4}, respectively. The green waveform is the current flow through an external short circuit current path applied in parallel with the switch S_2. The same current would flow through the switch S_1. The current is rising with the slope limited by the coupled inductor of qZSN. The transistors used in the experimental prototype are rated for the peak current of 100 A, which was not exceeded in healthy switches during

TABLE V
VOLTAGES ACROSS SWITCHES S_2 AND S_4 DURING NORMAL OPERATION

S_1	S_2	S_3	S_4	V_{S2}	V_{S4}
ON	OFF	OFF	ON	$V_{TX,pr}$	0
OFF	ON	ON	OFF	0	$V_{TX,pr}$
ON	ON	OFF	OFF	0	0
OFF	OFF	ON	ON	0	0

TABLE VI
VOLTAGES ACROSS SWITCHES DURING SHORT-CIRCUIT FAILURE

Fault	S_1	S_2	S_3	S_4	V_{S2}	V_{S4}
1	**SCF**	OFF	OFF	ON	$=V_{TX,pr}$	0
		ON	ON	OFF	0	$0\neq V_{TX,pr}$
2	ON	**SCF**	OFF	ON	$0\neq V_{TX,pr}$	0
	OFF		ON	OFF	0	$=V_{TX,pr}$
3	**SCF**	**SCF**	OFF	ON	$0\neq V_{TX,pr}$	-
			ON	OFF	-	$0\neq V_{TX,pr}$
4	**SCF**	OFF	**SCF**	ON	$0\neq V_{TX,pr}$	-
		ON		OFF	-	$0\neq V_{TX,pr}$
5	**SCF**	OFF	OFF	**SCF**	$=V_{TX,pr}$	-
		ON	ON		-	$0\neq V_{TX,pr}$
6	ON	**SCF**	OFF	**SCF**	$0\neq V_{TX,pr}$	-
	OFF		ON		-	$=V_{TX,pr}$

TABLE VII
MCU PARAMETERS RELATED TO FAULT IDENTIFICATION ROUTINE

Parameter	*Symbol*	*Value*
ADC sampling time, ns	samp. time	7.5
ADC resolution, bits	N_{RES}	12
ADC sample rate, kSamples/s	N_{SAPM}	400
Calculated measurement time, ns	t_{meas}	280
Time of fault detection routine, us	t_{handle}	1.7

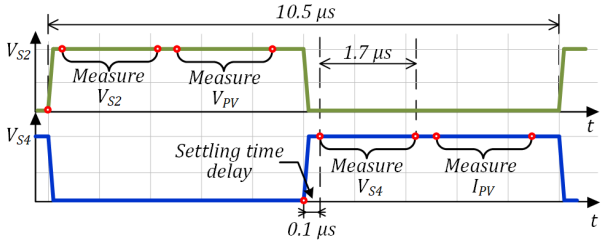


FIGURE 11. Synchronous measurement of parameters for fault detection.

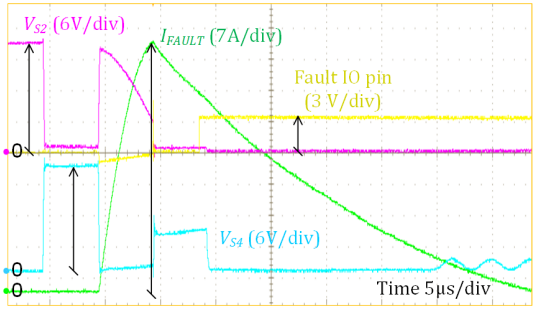


FIGURE 12. Experimental waveforms during fault detection of the proposed microconverter during SCF of the switch S_2.

the SCF detection delay. Purple waveform V_{S2} shows the discharge of the qZSN capacitors due to the SCF. The yellow waveform corresponds to an MCU output pin indicating when the control system has detected the SCF.

As a result, the proposed approach provides a low-cost fault detection implementation using simple resistive dividers as sensors and MCU ADCs at no extra cost. The fault detection is fast enough to prevent destroying healthy transistors from overtemperature or secondary breakdown. Converters for high voltage step-up applications often use overrated transistors to limit the conduction losses, which in combination with the current limiting features of the qZSN allow implementing the proposed low-cost fault detection.

When a fault is detected, the microconverter is turned off for a short time interval to make sure that all currents and voltages reach steady-state conditions. Then, a simple approach is employed for fault identification needed to select an appropriate post-fault modulation sequence. A simplified flowchart explaining the fault identification routine is presented in Fig. 13. The main principle is in the application of different switching vectors of 1.5 µs duration to the input-side bridge and further evaluation of converter response. The test starts with the input current measurement to check for non-recoverable short-circuit faults. In the figure, "Non reconf." corresponds to non-recoverable double faults.

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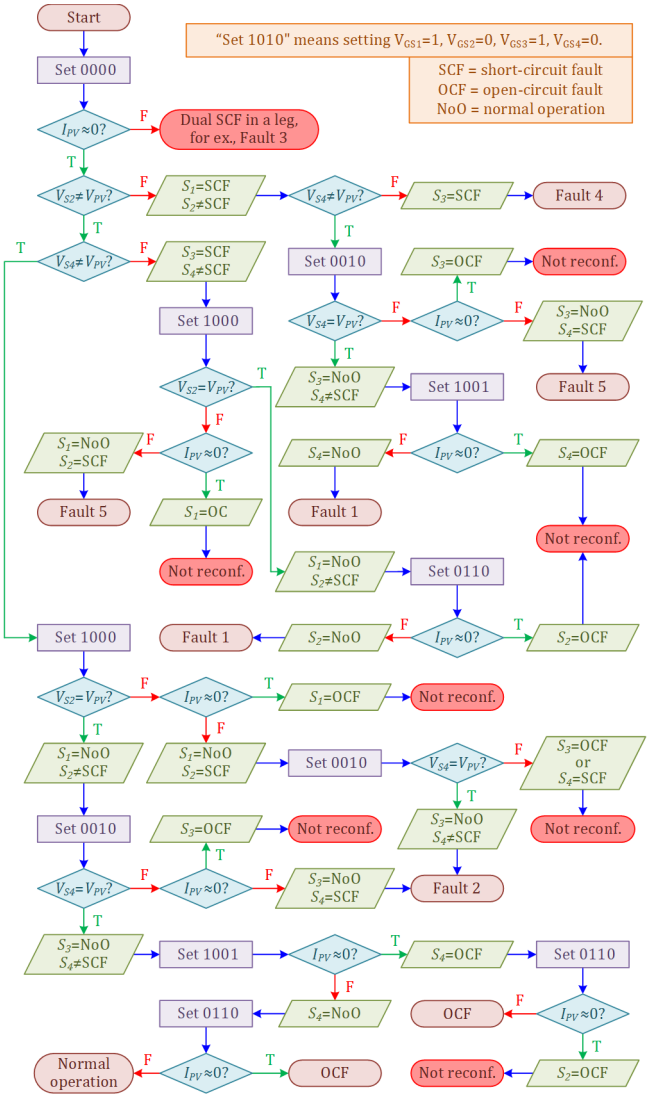


FIGURE 13. Simplified flowchart for identification of faults of the semiconductor switches according to Table VI.

VI. EVALUATION OF THE PERFORMANCE

In this section, the experimental performance benchmarking of the proposed FT-MIC is presented for the normal and post-fault operating scenarios.

A. POWER CONVERSION EFFICIENCY

The power conversion efficiency of the proposed FT-MIC was evaluated with the help of a precision power analyzer Yokogawa WT1800. In the first test the efficiency was measured at the boundary operating point $V_{PV,b} = 44$ V at different power levels from 10 to 100% of the rated value of 350 W. It is worth mentioning that in this point the converter operates as a series resonant DC transformer (like in Fig. 7*b*) thus demonstrating the highest power conversion efficiency. As it is seen from Fig. 14, during the normal operation, the proposed FT-MIC demonstrates the efficiency of over 96% in the range from 200 to 350 W with the peak value reaching 96.5% at 250 W. On the other hand, during the post-fault operation, the FT-MIC features the efficiency over 96% in the power range from 35 to 200 W achieving the peak value of 97.3% at 70 W.

Next, the California Energy Commission (CEC) weighted efficiency η_{CEC} was calculated as:

$$\eta_{CEC} = 0.04\cdot\eta_{10\%} + 0.05\cdot\eta_{20\%} + 0.12\cdot\eta_{30\%} + 0.21\cdot\eta_{50\%} + 0.53\cdot\eta_{75\%} + 0.05\cdot\eta_{100\%}, \quad (10)$$

where $\eta_{10\%}$, $\eta_{20\%}$, $\eta_{30\%}$, $\eta_{50\%}$, $\eta_{75\%}$, $\eta_{100\%}$ are the efficiency values measured at 10%, 20%, 30%, 50%, 75% and 100% of the rated power, correspondingly [10]. It is remarkable that having different power conversion efficiency profiles the FT-MIC during the normal and post-fault operation features almost identical CEC efficiency in the range from 95.5 % to 95.9 %.

Next, the efficiency variation over the predefined input voltage range of 15…65 V was evaluated. First, the efficiency curves shown in Fig. 15*a* were acquired for the FT-MIC operating with the predefined power envelope of the target operating range shown in Fig. 3*b*. In the next test, the efficiency was evaluated under the constant power operation at 120 W (Fig. 15*b*). The reconfigured converter has demonstrated excellent performance in the buck mode showing up to 3% better efficiency than in the normal operation.

The transition between the boost and buck regions was realized near the input voltage of 44 V. Therefore, an efficiency step of up to 7 % can be observed at this voltage in the post-fault operating conditions due to the change of the operating mode (Fig. 15). It was found that after the post-fault reconfiguration, the proposed FT-MIC was able to continue operation and ensure the demanded output voltage within the specified target operating range.

Based on the obtained results, it could be concluded that the microconverter could operate at higher light-load efficiency in the case of post-fault operation. Depending on the thermal design, power curtailment could be used when converter operates in the post-fault conditions and very high ambient temperature, or unusually high solar irradiance.

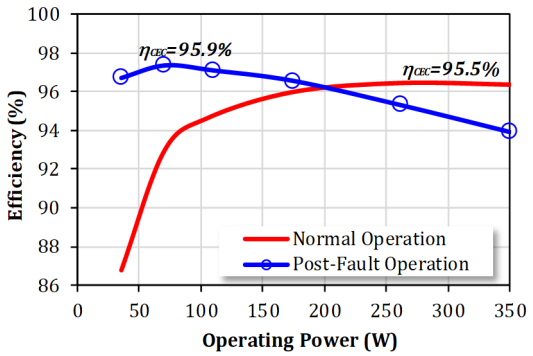


FIGURE 14. Evaluation of California Energy Commission (CEC) weighted efficiency of the proposed FT-MIC during the normal and post-fault operation at $V_{PV,b}$ = 44 V.

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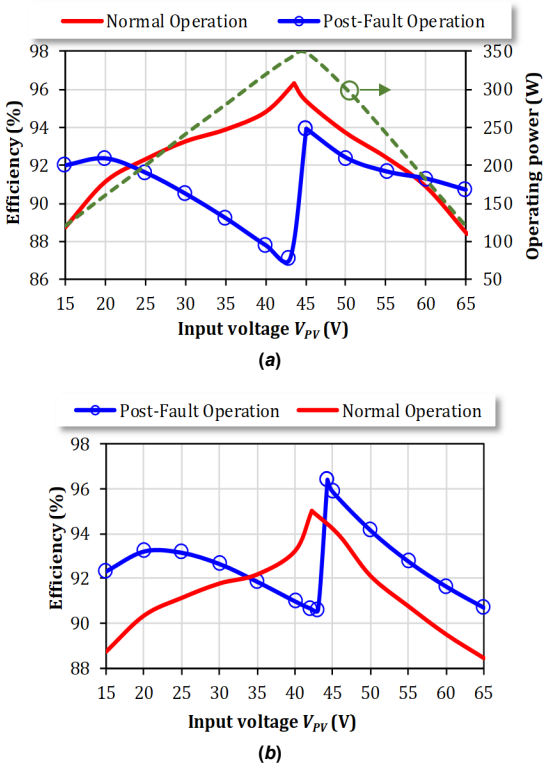


FIGURE 15. Experimental power conversion efficiencies of the proposed FT-MIC during the normal and post-fault operation for the predefined variable power envelope shown in Fig. 3*b* (*a*) and at constant power of 120 W (*b*).

B. MPPT PERFORMANCE

The study of the MPPT performance is based on a physical model of the polycrystalline Si-based PV module Solar Innova SI-ESF-M-P125-96 that contains 96 typical PV cells. It features the nameplate power rating of 275 W. Fig. 16 show example of its characteristics that correspond to the Nominal Operating Cell Temperature (NOCT) conditions: solar irradiance of 800 W/m^2, air temperature of 20 °C, the air quality of 1.5, wind speed of 1 m/s, and PV cell temperature of 47 °C [37]. This corresponds to the target operating range of the proposed FT-MIC and illustrates the transition between the modes in the post-fault conditions.

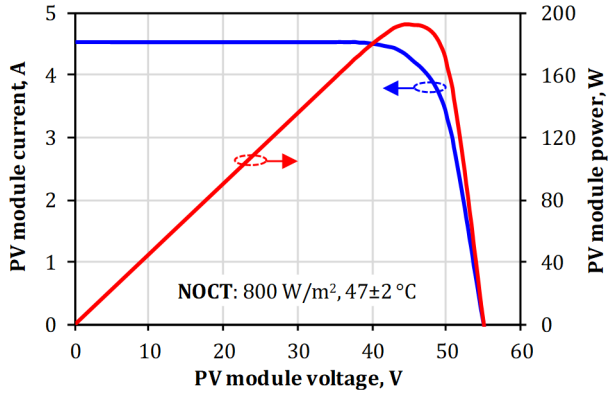


FIGURE 16. I-V and P-V characteristics of the case study PV module in the NOCT conditions.

The experimental setup shown in Fig. 17 was used in this and the next subsections. It contains solar array simulator (SAS) Keysight E4360A, device under test (FT-MIC prototype from Fig. 3*a*), and programmable DC load Chroma 63204 that was set up for constant voltage mode at the typical voltage of the residential DC microgrids of 350 V.

The sketch of the control system that implements the MPPT functionality along with the fault detection and identification is shown in Fig. 18. These two algorithms are decoupled, and the MPPT is executed until a fault is detected. The MPPT block utilizes a simple incremental conductance algorithm for generating the reference voltage. The PI controller ensures that the converter reaches the new reference point. The output of the PI controller is bipolar to implement the multi-mode control principle: positive output is used as the boost mode control variable, while the absolute value of the negative output signal is translated into the buck mode control variable, like in [8].

Once a fault is detected, the fault detection block changes its status output (inverse "Fault" signal), which results in disabling the main pulse-width modulator by changing the output of the XNOR block. Next, the fault identification block takes over the control of the gating signals. It performs a fault search algorithm by directly setting different switching vectors to the corresponding input/output (IO) pins of the microcontroller, according to the flowchart from Fig. 13. When the fault is identified, this block provides a fault code to the main modulator for reconfiguration of modulation sequences and enables the modulator through the XNOR block by setting the status output (inverse "Post-fault" signal) to the low level. After that, the MPPT routine can be restarted using the recovered converter. The NOR gate defines operation of the switch/relay S_R.

The MPPT is an important part of the closed-loop control system in any PV microconverter. The capability of the FT-MIC to track the maximum power point under any conditions is of superior importance. The FT-MIC prototype was configured to first operate in the normal and then in the post-fault conditions. During the test, the SAS was emulating the I-V profile from Fig. 16. It could be observed from Fig. 19 that the MPPT routine performed in the normal conditions (Fig. 19*a*) and in the post-fault conditions (Fig. 19*b*) are similar in dynamic performance. There are two main differences observed in the post-fault conditions comparing to the normal conditions: the transformer voltage becomes

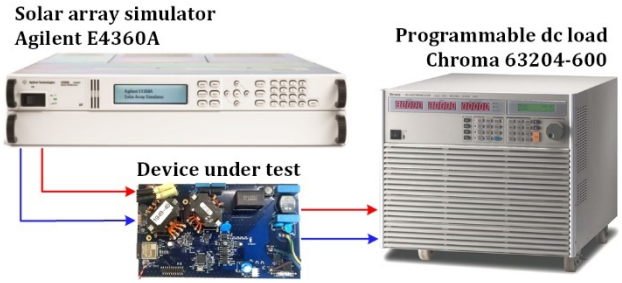


FIGURE 17. Experimental setup for MPPT performance evaluation.

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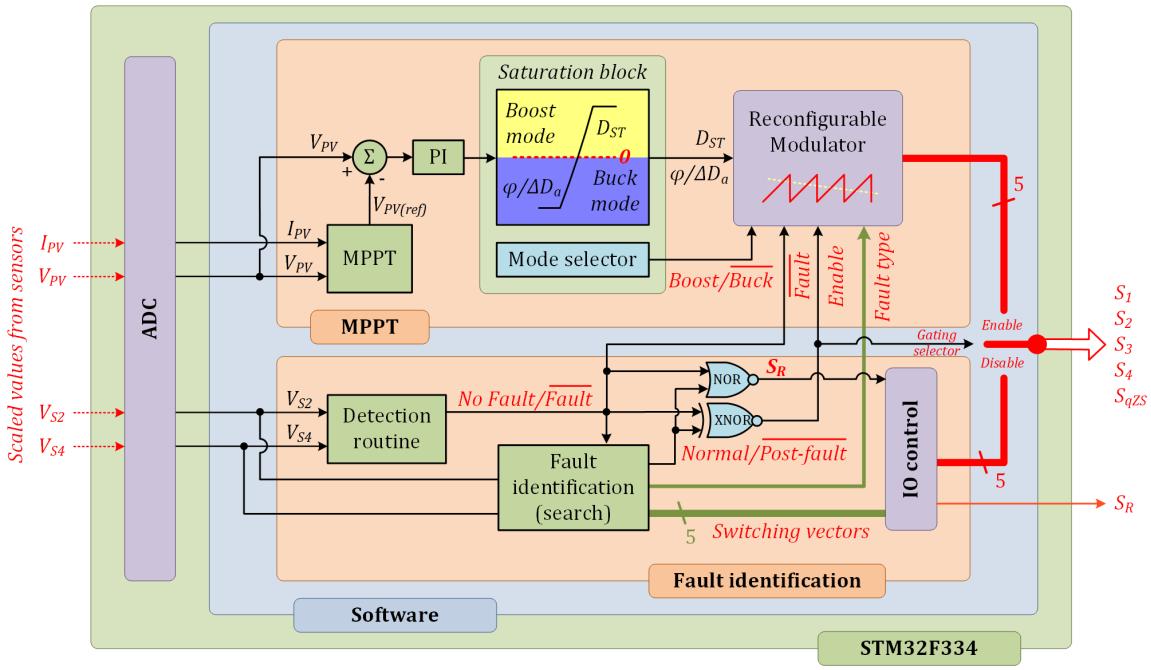


FIGURE 18. Simplified sketch of the closed-loop control system.

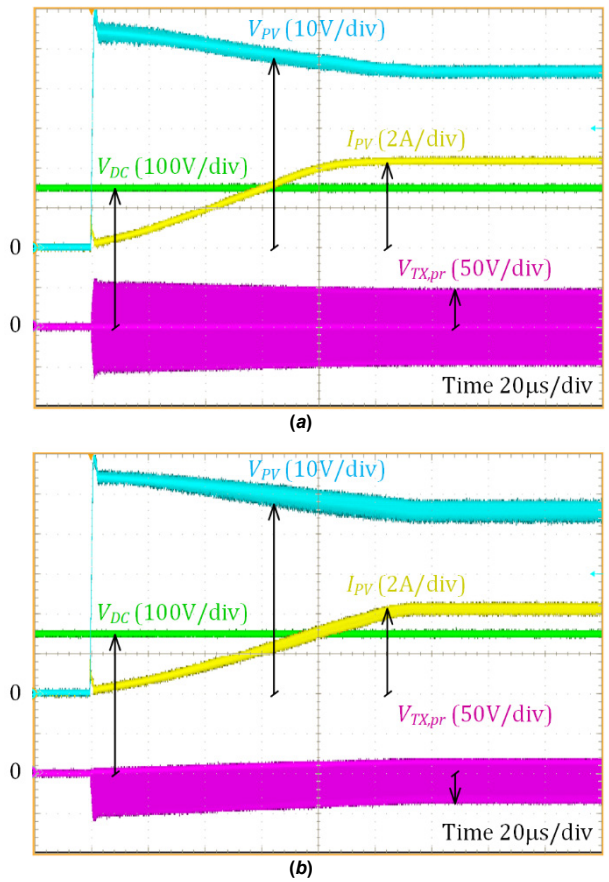


FIGURE 19. Experimental MPPT routine performed by FT-MIC in the normal (*a*) and post-fault (*b*) conditions with the I-V profile from Fig. 16.

asymmetrical; the input voltage ripple is increased as the converter input current ripple has two times lower equivalent frequency. Other than those changes, the converter can perform MPPT in roughly 120 ms.

C. DAILY PV ENERGY YIELD TEST

This section describes how the proposed FT-MIC can handle the long-term PV energy generation test. The daily profile of the solar irradiance and the corresponding PV cell temperature used in this subsection is presented in Fig. 20. The considered conditions correspond to a sunny summer day in the Northern European mild climate zone. The PV cell temperature experiences the temperature swing of over 40 °C, which results from roughly 20 °C daily ambient temperature swing, and PV module heating by the sunlight. The peak solar irradiance of 800 W/m^2 is typical for the given geographical region.

The daily mission profile from Fig. 20 was emulated for the case study 96-cell PV module by the SAS. A custom-made LabVIEW application was used to implement the SAS control with the resolution of one second for the mission profile and measurements. Additionally, the measured data were logged by the precision power analyzer WT1800. The experimental results for the normal and post-fault operating conditions are presented in Fig. 21*a* and 21*b*, respectively.

Fig. 21 presents (from top to bottom): input voltage of the FT-MIC prototype, input (P_{PV}) and output (P_{DC}) powers of the prototype, MPPT efficiency (ratio between intravenous values of the available and extracted PV power), and the prototype electric power conversion

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efficiency. In both conditions, the prototype could extract roughly 1190 Wh of the energy from the SAS. The average MPPT efficiency in both cases was over 99 %. Hence, the main difference in results is associated with the power stage efficiency.

In the normal operating conditions, the prototype was approaching maximum efficiency of 95 %, as shown in Fig. 21*a*. As predicted, the peak efficiency was observed at the maximum input power, i.e., the highest solar irradiance of 800 W/m^2. The daily energy yield of 1116 Wh was measured at the converter output, which corresponds to 93.8 % of 1190 Wh, the energy extracted from the SAS.

In the post-fault operating conditions, the prototype shows good MPPT performance, as shown in Fig. 21*b*. As the maximum power point voltage drops when the PV cell temperature is rising, the converter automatically changes its operating mode from the buck mode to the boost mode between the fourth and seventh hours. In the boost mode, the converter power loss is increased by roughly two times, which is evident from the drops in both the experimental efficiency curve and the input and output power curves. In the given case study conditions, the output energy yield drops down to 1070 Wh, which corresponds to 89.9 % of the energy received at the prototype input terminals. Therefore, the prototype would be losing an extra 3.9% of the input energy if it was recovered after a semiconductor switch fault. This is an acceptable performance deterioration, considering that the FT-MIC can continue operation after a semiconductor switch fault.

VII. CONCLUSION

This paper proposes the adoption of the high regulation flexibility of the qZS series resonant DC-DC converter for fault-tolerant application. It was proposed and verified that the converter can sustain its operation after a fault in one of the front-end inverter transistors, and several cases of double faults. Moreover, it remains capable of operating in the wide input voltage range from 15 V to 65 V due to buck-boost voltage regulation functionality, which makes it compatible with most of the typical PV modules available on the market. The low-cost implementation of a fault detection using simple voltage dividers and ADCs embedded in a microcontroller was proposed and experimentally validated. The quasi-Z-source network limits the fault currents in healthy switches and allows for withstanding the maximum delay between a fault and converter shut down of less than a switching period. Besides, a simple fault identification based on the sequential application of switching vectors to the input-side bridge was proposed. As a result, a low-cost fault-tolerant PV microconverter was implemented.

Experimental verification of the microconverter performance showed that it has higher efficiency at the full load in the normal operation, and at a light load in the post-fault operation conditions. The peak efficiency of over 95 % was achieved in both cases. It was also demonstrated that the dynamic and static MPPT performances of the microconverter does not deteriorate after a fault and converter can track a maximum power point with over 99% accuracy. The daily PV energy production was also emulated for the case of 96-cell Si-based PV module in both normal and post-fault operating conditions. The microconverter was able to deliver 93.8 % of the harvested PV energy to the output in the normal operation, and 89.8 % in the post-fault operation. Drop in the energy production is a result of considerable efficiency step when the microconverter switches between the buck and the boost modes. Nevertheless, it is an acceptable tradeoff considering possible lifetime extension.

The proposed idea of fault-tolerant PV microconverter could help to realize the deferred maintenance approach resulting in reduced downtimes and faster return of investments of the residential PV power systems. The future research will focus on damage accumulation rate in the microconverter components in the normal and post-fault operation and their comparison and optimization via hardware design tailoring.

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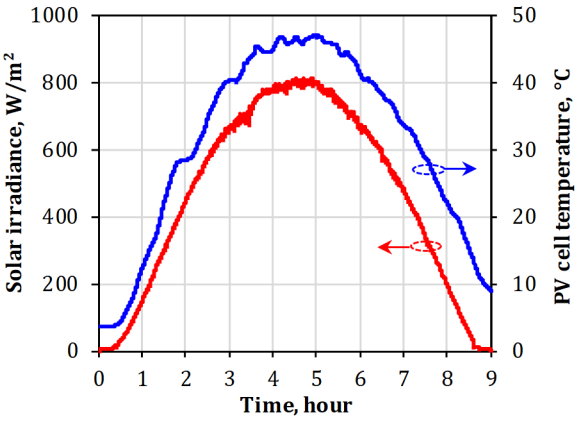


FIGURE 20. Case study daily profile of solar irradiance and estimated PV cell temperature.

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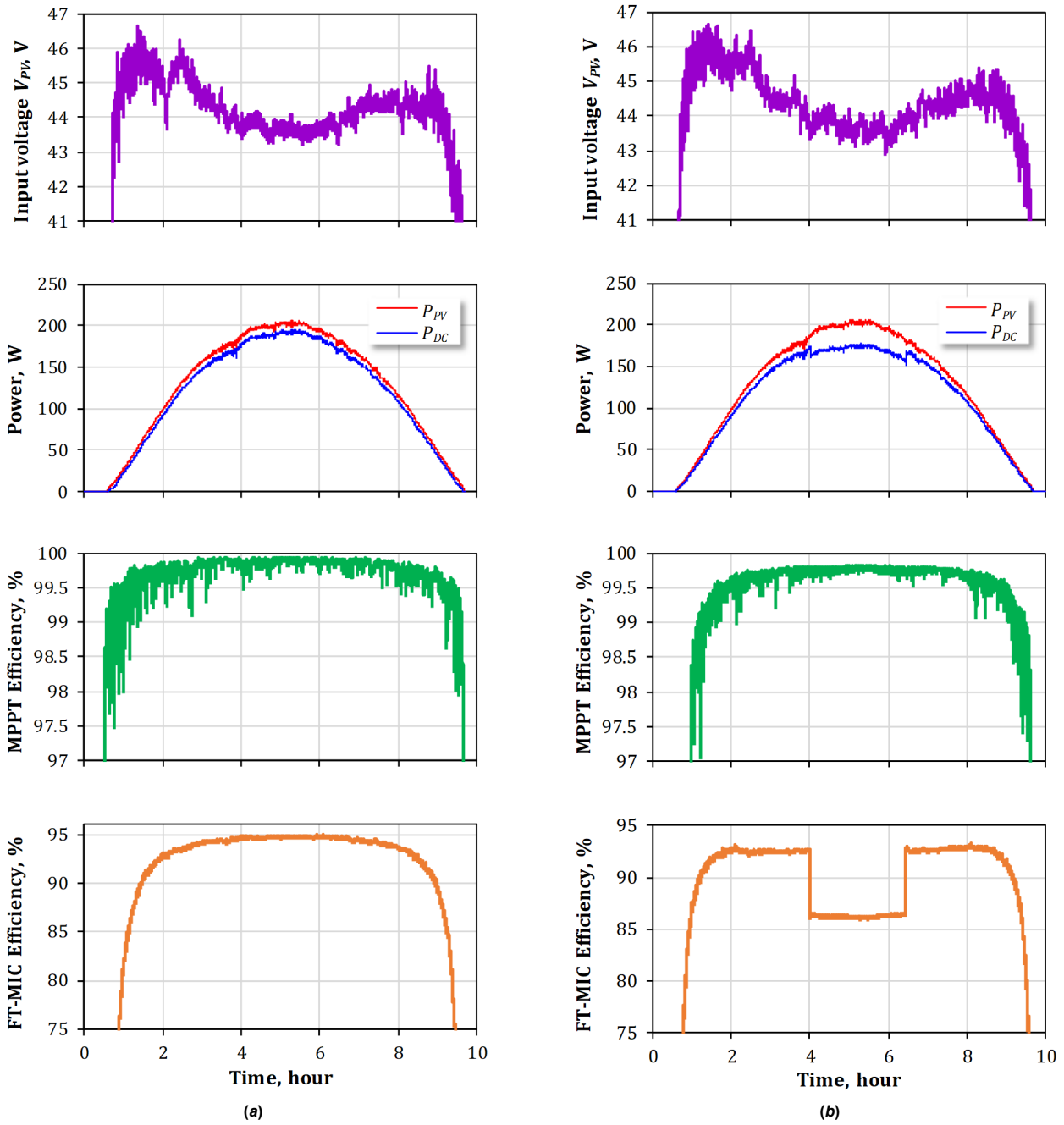


FIGURE 21. Experimental results of the daily PV energy generation test performed by the FT-MIC prototype in the normal (*a*) and post-fault (*b*) operating conditions.

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